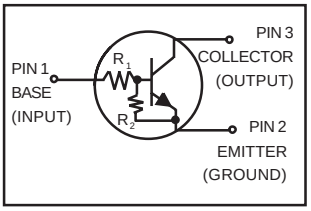
Bias Resistor Transistor
NPN Silicon Surface Mount Transistor
with Monolithic Bias Resistor Network

LMUN5236T1G
S-LMUN5236T1G

SC-70 / SOT-323



●FEATURES

1)Simplifies Circuit Design
2)Reduces Board Space and Component Count
3)We declare that the material of product compliant with RoHS requirements and Halogen Free.
4)S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

●DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LMUN5236T1G	8N	3000/Tape&Reel
LMUN5236T3G	8N	10000/Tape&Reel

●MAXIMUM RATINGS(Ta = 25℃)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Collector Current	I_C	100	mA

●THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Total Power Dissipation @Ta = 25°C Derate above 25°C	P_D	202(Note 1.) 310(Note 2.) 1.6(Note 1.) 2.5(Note 2.)	mW °C/W
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	618(Note 1.) 403(Note 2.)	°C/W
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	280 (Note 1) 332 (Note 2)	°C/W
Operating and Storage Temperature Range	Topr, Tstg	–55 to +150	°C

1. FR–4 @ Minimum Pad

2. FR–4 @ 1.0 x 1.0 inch Pad.

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●ELECTRICAL CHARACTERISTICS (Ta= 25℃)

OFF CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-Base Cutoff Current	I_{CBO}	–	–	100	nA	V_{CB} = 50 V, I_E = 0
Collector-Emitter Cutoff Current	I_{CEO}	–	–	500	nA	V_{CE} = 50 V, I_B = 0
Emitter-Base Cutoff Current	I_{EBO}	–	–	0.05	mA	V_{EB} = 6.0 V, I_C = 0
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	50	–	–	V	I_C = 10 μA, I_E = 0
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	50	–	–	V	I_C = 2.0 mA, I_B = 0

ON CHARACTERISTICS(Note2.)

DC Current Gain	h_{FE}	80	150	–		V_{CE} = 10 V, I_C = 5.0 mA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	–	–	0.25	V	IC = 10 mA, IB = 0.3 mA
Output Voltage (on)	V_{OL}	–	–	0.2	V	VCC = 5.0 V, V_B = 5.5 V, R_L = 1.0 k Ω
Output Voltage (off)	V_{OH}	4.9	–	–	V	V_{CC} = 5.0 V, V_B = 0.5 V, RL = 1.0 k Ω
Input Resistor	R1	70	100	130	k Ω	
Resistor Ratio	R1/R2	0.8	1	1.2		

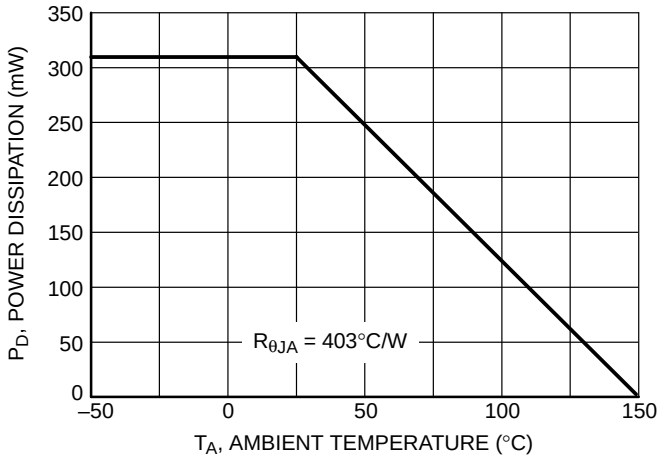

FIG.1 Derating Curve

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ELECTRICAL CHARACTERISTIC CURVES

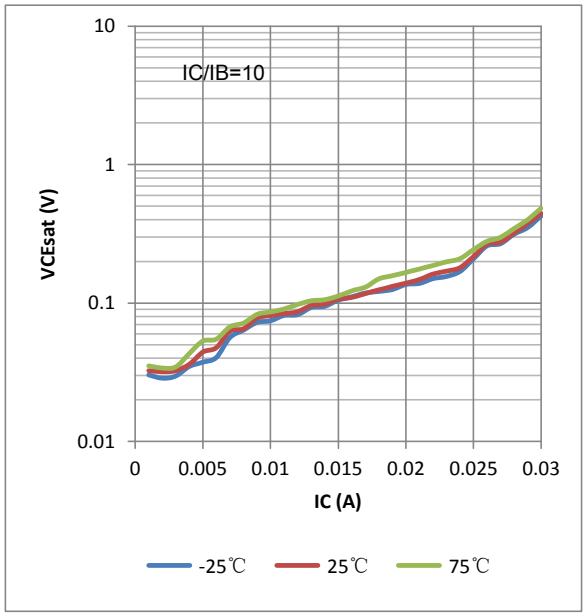

FIG.2 $V_{CE\ (sat)}$ vs. I_C

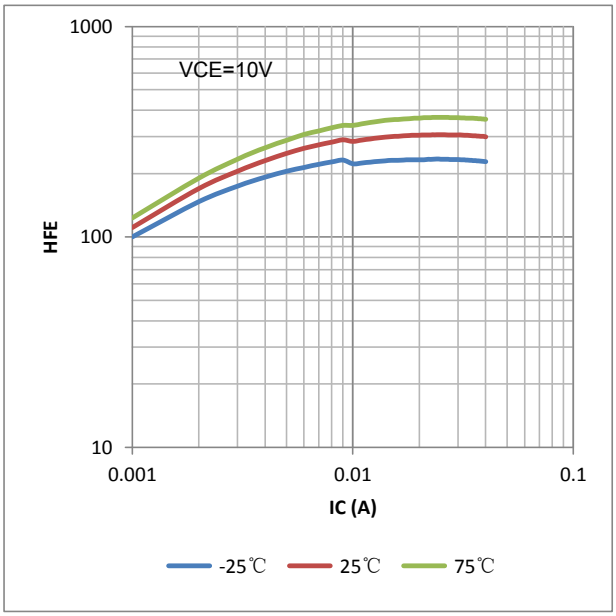

FIG.3 DC Current Gain

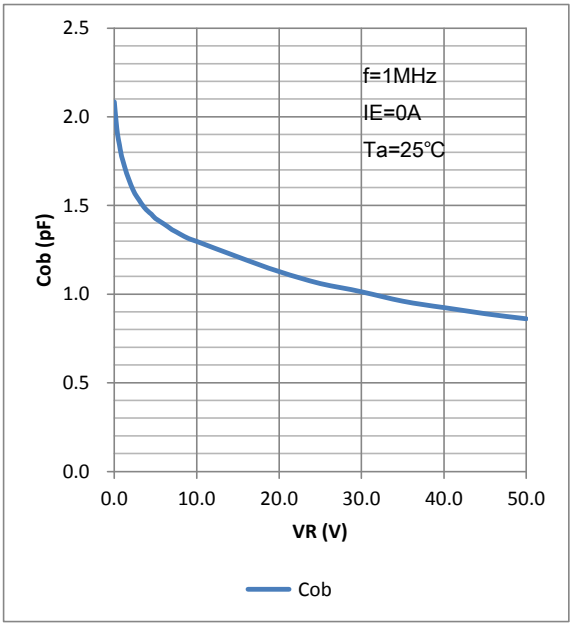

FIG.4 Output Capacitance

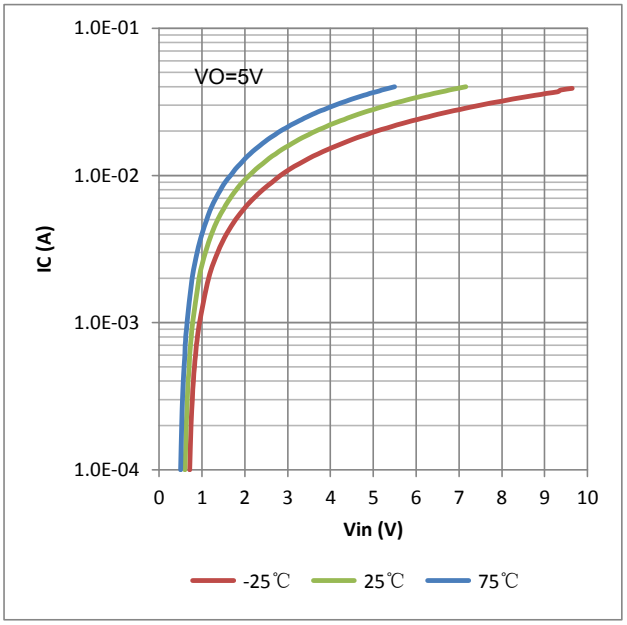

FIG.5 Output Current versus Input Voltage

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ELECTRICAL CHARACTERISTIC CURVES

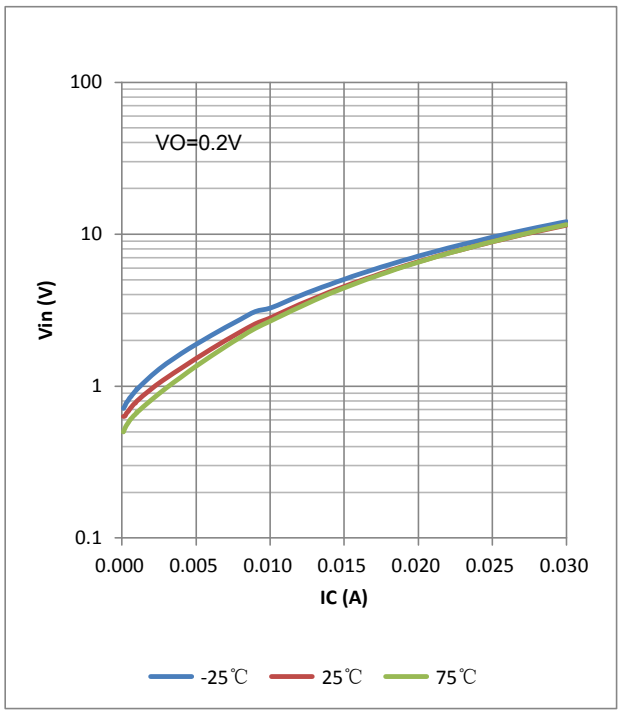

FIG.6 Input Voltage vs. Output Current

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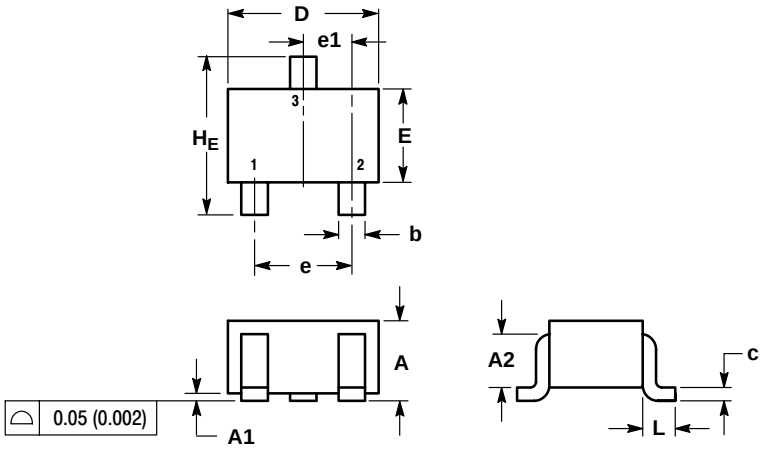
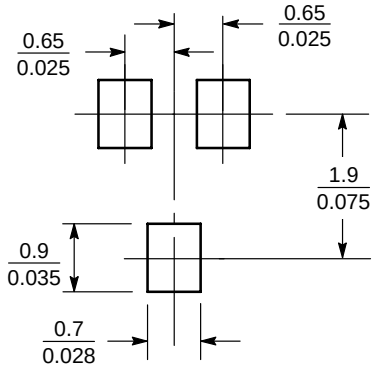


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

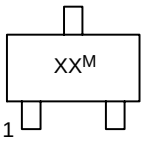
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.7 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L		0.425 REF			0.017 REF	
H_E	2.00	2.10	2.40	0.079	0.083	0.095

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{mm}{inches}\right)$

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.