OUTLINE
DIGITAL POTENTIOMETERS

What is digital potentiometer?

Digital potentiometers are variable resistors that can adjust freely setting values by external digital signals. Further, these have the same functions as mechanical potentiometers by writing setting values stored when nonvolatile EEPROM memory is written and electricity is ON. Especially, the latest product series achieve low power consumption and operation currents realize 1mA and standby currents 1 μA.
Standard features are the following:

- Without moving parts, environmental characteristics have been improved.
- Remote control of the product is possible by digital signals.
- Without moving parts, there are absolutely no hysteresis.
- Automatic adjustment makes it possible to reduce numbers of adjustment processes.
- Space-conscious packages available.

On the contrary, there are some disadvantages in digital potentiometers. Different from mechanical potentiometers, the wiper of the digital potentiometers operates like steps. The numbers of the type of total resistance values are few. Temperature characteristics are inferior. Because of its structure of CMOS circuitry used for a wiper changeover switch, frequency characteristics are also inferior to mechanical potentiometers. Other disadvantages include weakness for over-voltage and over-current.

Digital potentiometers are categorized by control types and their features as below.

- Up/down interface type
  - 3 control signals control wiper position ($U/\overline{D}$, $\overline{INC}$, $\overline{CS}$)
  - For wiper positions (number of taps), 32 and 100 types are available.

- 2-wire interface type
  - Uses 2-wire serial interface
  - Resistor system permits direct reading of wiper position and setting.
  - Multiple circuits are built into one chip (2-circuit or 4-circuit).
  - Wiper position of 64 or 128 and 256 taps per circuit

- SPI interface type
  - Resistor system permits direct reading of wiper position and setting.
  - Multiple circuits are built into one chip (2-circuit or 4-circuit).
  - Wiper position of 64 or 256 taps per circuit
  - It operates at 3 Mbps faster than 2-wire interface type

- 3-wire interface type
  - 3-wire of CLK, DI, and CS controls by serial interface

GLOSSARY
DIGITAL POTENTIOMETERS

● Nominal resistance value
Nominal resistance value is the value between terminal V_H and V_L of potentiometers. It depends on each series and in digital potentiometers, it ranges from 1 kΩ to 100 kΩ.

● Maximum input voltage
Maximum input voltage is the maximum voltage that can impress between terminals, V_H and V_L. It can impress up to Vcc voltage.

● Maximum wiper current
This is the maximum current sent to wiper. One of the specifications to be noted in the digital potentiometer is that current is from ± 0.6 mA to ± 6 mA.

● Number of taps (Resolution)
Resolution in cermet trimmer is logically infinitesimal. But, in digital potentiometers, resistance values will change in a step state at 16 ~ 256 taps, and not linearly.

● Rated power
Rated power is the maximum power that potentiometers can consume under prescribed condition, while they are satisfying requested performances.

● Resistance temperature characteristics
Resistance temperature characteristics mean changing ratios of total resistance when environmental temperatures change. Resistance temperature coefficient is a unit of one millionth per 1 °C (10^{-6}/°C) (ppm/°C)

Resistance temperature characteristics

$$(10^{-6}/°C) = \frac{R - R_0}{R_0} \times \frac{1}{t - t_0} \times 10^6$$

R : Actual resistance measurement value (Ω) at t °C
R_0: Actual resistance measurement value (Ω) at t_0 °C
t : Actual measurement value (°C) of test temperature
t_0: Actual measurement value (°C) of standard temperature

Resistance temperature characteristics are largely affected by materials contents of resistance elements. Resistance temperature characteristics of the digital potentiometers are relatively large compared with commonly used potentiometers, in the order of hundreds 10^{-6}/°C in minus side.

GLOSSARY
DIGITAL POTENTIOMETERS

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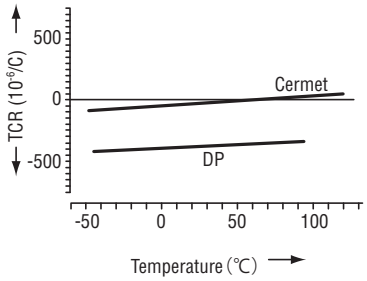

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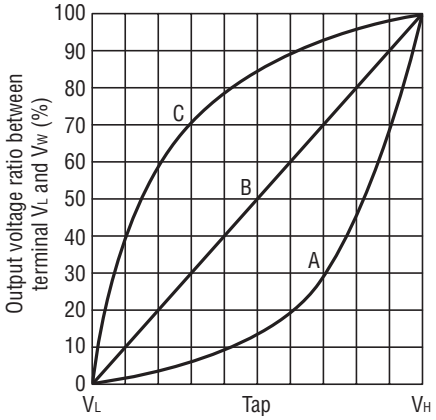
● Resistance law

When voltage is added between V_H and V_L and wiper is moved either from V_L to V_H or from V_H to V_L, resistance law is divided into several types depending on conditions of output voltage ratio between terminal V_L and Vw or Vw and V_H. Typically, there are three types (A, B, and C) as Fig. shows. In case of digital potentiometers, actual resistance shows step-like change. In digital potentiometers, there are 3 types of either A or B or C.



● Package

Package is a shape of IC. In digital potentiometers, there are 6 different types.
SOIC: Small Outline Integrated Circuit
MSOP: Miniature Small Outline Package
TSSOP: Thin Small Surface Outline Package
TDFN: Thin Dual Flat Non-Lead Package
SOT-23: Small Outline Transistor
SC70: Single Chip

● Latch-Up

Latch-up is a phenomenon that exists in circuits fabricated using CMOS. As far as CMOS elements are used within maximum rated voltage, there will be no damages or problems. By exceeding maximum rated voltage or current to each terminal, latch-up phenomenon occurs by short-circuiting between power supply and ground and may lead to element destroy.

● Resistor

Resistor is a small capacity memory to save data such as wiper position.

GLOSSARY
DIGITAL POTENTIOMETERS

● Wiper resistance
MOS FET channel resistance is linearly placed in wiper terminal to change wiper taps. This figure differs from 50 to 1 kΩ depending on types and increases with temperature.

● Wiper noise
Basically, wiper noise will not be generated as much as when writing in memories. Since Make-Before-Break operation is used and change-over noise is depressed, Total resistance value will be temporarily going down. This means that new wiper tap is made before breaking.

● Wiper current leakage
While digital potentiometer is in operation, 100 nA typ current leakage will be generated from wiper to Vss.

● 2-wire interface
This 2-wire interface is the interface controlled by two signal lines of serial data and serial clock, allowing it to minimize wiring to microcomputer.

● CMOS
CMOS is an abbr. of Complementary Metal Oxide Semiconductor. CMOS is a widely used type of semiconductor. This CMOS semiconductor incorporates both P-channel and N-channel FET within one chip and makes them complementary. CMOS IC is currently a mainstream of LSI, requiring very low power and allowing high-speed operation. On the contrary, it has a disadvantage to be easily broken by static electricity and others.

● E^2PROM
Short term for Electrically Erasable Programmable Read-Only Memory. EEPROM is a nonvolatile memory that can rewrite contents electrically and incorporates pressure circuitry of voltage necessary for writing or erasing cells. Rewriting numbers of times of EEPROM is 1 million times in the DP series. Written data can be stored for 100 years.

● ESD
ESD is an abbreviation of Electrostatic Discharge. As the advance of miniaturization for the semiconductor,the semiconductor devices become vulnerable to ESD. The deterioration and the injury of the device by ESD become very important problem.

● Icc
Icc is a consumption current while digital potentiometer is in operation, when wiper position is changed or at writing data. (Icc1: Consumption current at change of wiper position. Icc: Consumption current at writing data.)

● Isb
Isb is a consumption current when wiper position is unchanged while digital potentiometer is in operation.

● MIL
Military Industrial Law (MIL) is the U.S. military standard. Since this standard is standardized and commercially available, you can get information via internet.

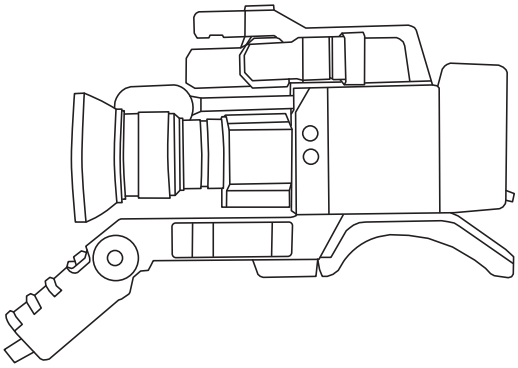
● SPI interface
SPI interface is the type of interface controlled by 3-wire of SCK, SI and CS. It can operate at 3 Mbps faster than 2-wire interface.

● Vcc (Power supply)
Supply voltage: 2.5 ~ 6.0 V / 2.5 ~ 5.5 V / 2.7 ~ 5.5 V

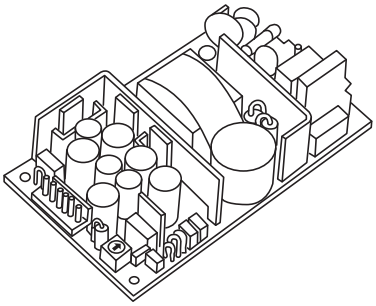
APPLICATIONS
DIGITAL POTENTIOMETERS

< Communications equipment >
- Cell phones
- Exchangers
- Facsimile
- Assorted wireless equipment
- MUX

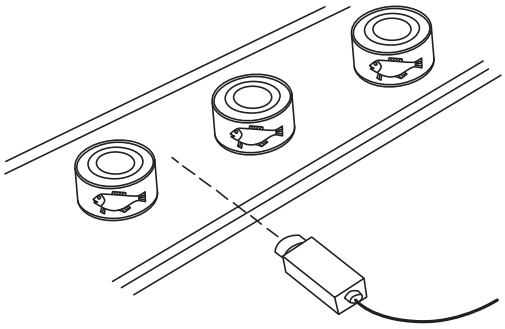
< Broadcasting equipment >
- Professional use camcorders
- Color monitors
- VTR equipment



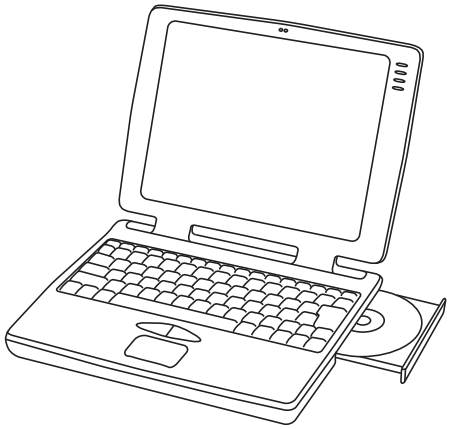
< Power supply equipment >
- Switching power supplies
- DC electrical power source equipment
- Assorted power supply circuits
- Battery changers



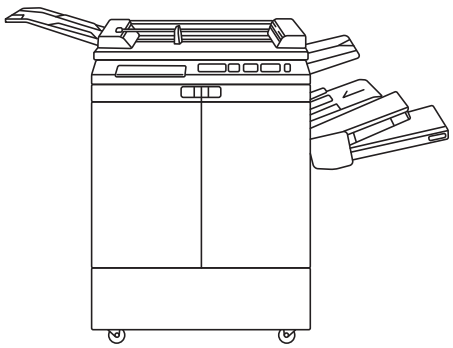
< Sensor devices >
- Photoelectric sensors
- Pressure sensors
- Encoders
- Magnetic sensors



< Computer and peripherals >
- Laser beam printers
- Displays
- Notebook computers
- Projectors



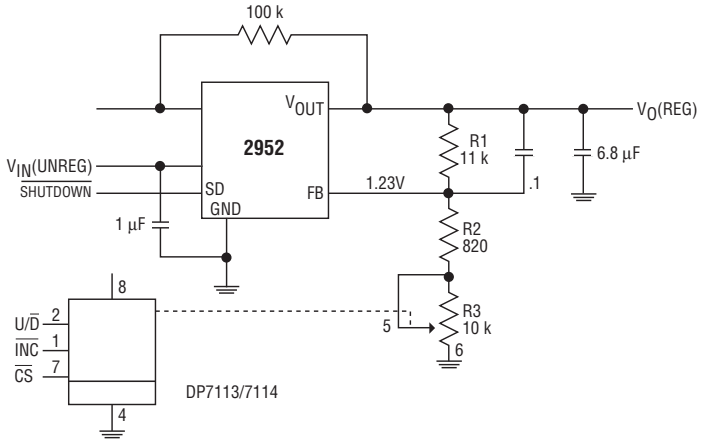
< Others >
- Hematology analyzers
- PPC/Multifunction machines
- TV
- Programable controllers
- Robots



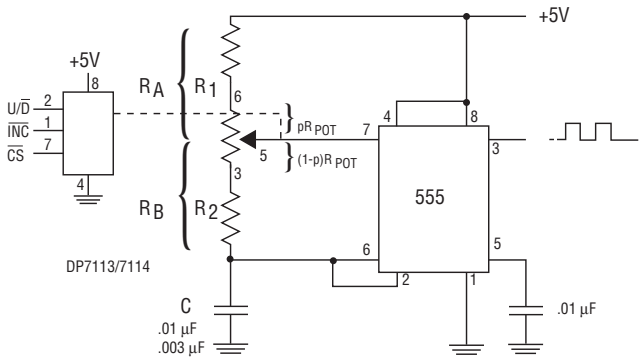
APPLICATIONS
DIGITAL POTENTIOMETERS

< Basic configurations of electronic potentiometers >

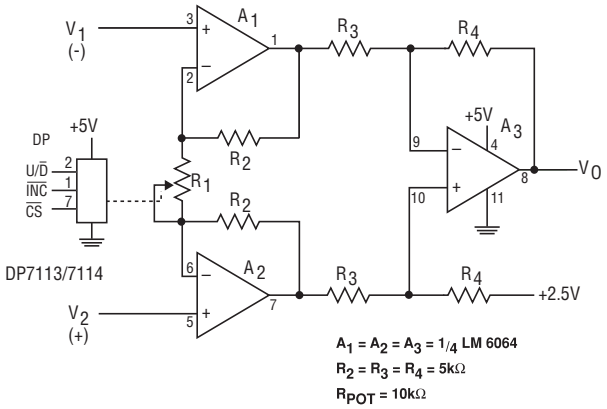
● **Programmable Voltage Regulator**



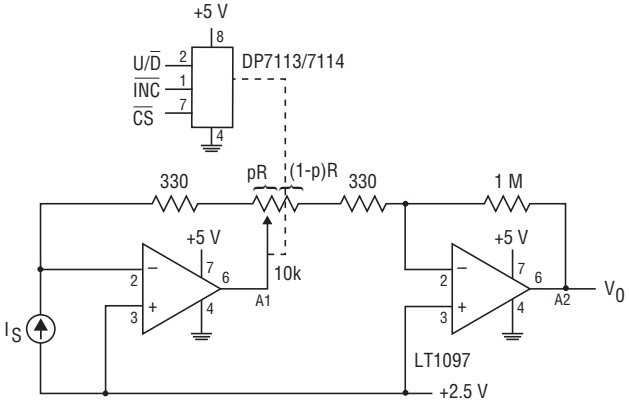
● **555 IC Oscillator**



● **Programmable Instrumentation Amplifier**



● **Programmable I to V convertor**



DP series
DIGITAL POTENTIOMETERS

■ LIST OF PART NUMBERS

Product number	Pot	Tap	(V) Power supply voltage	(kΩ) * Total resistance value	I/F	(Hz) Clock frequency	(Ω) Wiper resistance	(mA) Wiper current	Package *	Note
DP7112	1	32	2.5-6.0	10, 50, 100	U/$\overline{D}$	1 M	—	—	8MSOP/8SOIC/8TSSOP	With buffer
DP7114	1	32	2.5-6.0	10, 50, 100	U/$\overline{D}$	1 M	400@2.5 V/200@5 V	± 4.4	8TDFN/8MSOP/8SOIC/8TSSOP	
DP7115	1	32	2.5-5.5	10, 50, 100	U/$\overline{D}$	1 M	400@2.5 V/200@5 V	1	8MSOP/8SOIC/8TSSOP	Volatile
DP7111	1	100	2.5-6.0	10, 50, 100	U/$\overline{D}$	1 M	—	—	8MSOP/8SOIC/8TSSOP	With buffer
DP7113	1	100	2.5-6.0	1, 10, 50, 100	U/$\overline{D}$	1 M	1k@2.5 V/400@5 V	± 4.4	8MSOP/8SOIC/8TSSOP	
DP7221	2	64	2.5-6.0	2.5, 10	2W	400 k	300@3 V/150@5 V	± 6	20TSSOP	
DP7411	2	64	2.5-6.0	10, 50, 100	SPI	3 M	300@3 V/150@5 V	± 6	24TSSOP	
DP7419	2	64	2.5-6.0	10, 50	2W	400 k	300@3 V/150@5 V	± 6	24TSSOP	
DP7261	2	256	2.5-6.0	50, 100	SPI	3 M	300@3 V/150@5 V	± 6	24TSSOP	
DP7269	2	256	2.5-6.0	50 ,100	2W	400 k	300@3 V/150@5 V	± 3	24TSSOP	
DP7241	4	64	2.5-6.0	2.5, 10, 50, 100	2W	400 k	300@3 V/150@5 V	± 6	20TSSOP	
DP7401	4	64	2.5-6.0	2.5, 10	SPI	3 M	300@3 V/150@5 V	± 6	24TSSOP	
DP7409	4	64	2.5-6.0	10, 50, 100	2W	400 k	300@3 V/150@5 V	± 6	24TSSOP	
DP7251	4	256	2.5-6.0	50, 100	SPI	3 M	300@3 V/150@5 V	± 6	24TSSOP	
DP7259	4	256	2.5-6.0	50, 100	—	400 k	300@3 V/150@5 V	± 3	24TSSOP	
DP7120	1	16	2.7-5.5	10, 50	U/D	1 M	600@2.7 V	± 1.3 (10, 50 kΩ)	6SC70/6SOT-23	Volatile
DP7121	1	16	2.7-5.5	10, 50	U/D	1 M	600@2.7 V	± 1.3 (10, 50 kΩ)	6SC70/6SOT-23	Volatile
DP7122	1	16	2.7-5.5	10, 50	U/$\overline{D}$	1 M	600@2.7 V	± 1.3 (10, 50 kΩ)	5SC70/5SOT-23	Volatile
DP7110	1	32	2.7-5.5	10, 50, 100	U/$\overline{D}$	1 M	600@2.7 V	± 1.3 (10, 50 kΩ)/± 0.6 (100 kΩ)	6SC70/6SOT-23	Volatile
DP7118	1	32	2.7-5.5	10, 50, 100	U/$\overline{D}$	1 M	600@2.7 V	± 1.3 (10, 50 kΩ)/± 0.6 (100 kΩ)	5SC70/5SOT-23	Volatile
DP7119	1	32	2.7-5.5	10, 50, 100	U/$\overline{D}$	1 M	600@2.7 V	± 1.3 (10, 50 kΩ)/± 0.6 (100 kΩ)	6SC70/6SOT-23	Volatile
DP7132	1	128	2.7-5.5	10, 50, 100	2$\overline{W}$	400 k	200@8 V/150@12 V	± 3	10MSOP	Pot voltage 8 ~ 16 V
DP7140	1	256	2.5-5.5	50	2$\overline{W}$	400 k	200@3.3 V	± 3	8MSOP	
DP7172	1	256	2.7-5.5	50, 100	SPI	25 M	250@3 V/120@5V	± 3	8SOT-23	Volatile

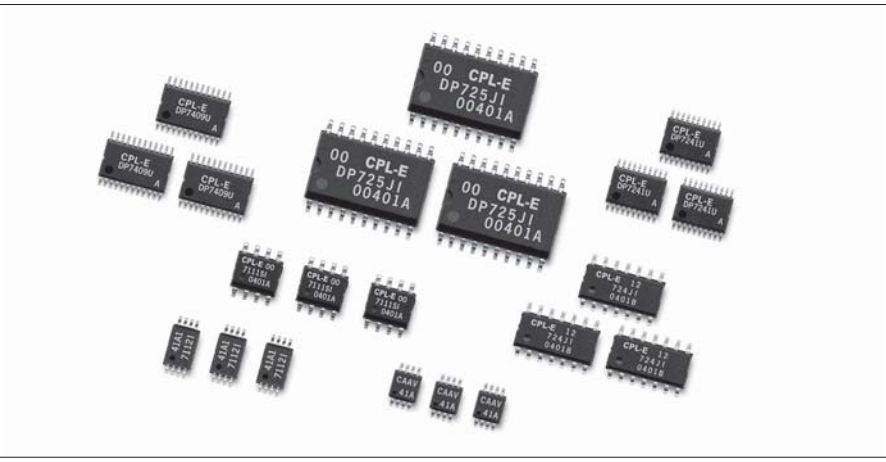
Legend Pot : No. of poteniometer Tap : No. of taps I/F : Interface type U/$\overline{D}$: UP/DOWN SPI : Serial Peripheral Interface 2W : 2-wire interface

* Resistance value will vary depending on the package. For details, please contact us.

Copal DP	Development Support Kit for DP

DIGITAL POTENTIOMETERS

DP 7114



FEATURES

- 32-position, linear-curved potentiometer
- Nonvolatile memory wiper storage
- Low-power CMOS technology
- Single-power operation: 2.5 V ~ 6.0 V
- Increment up/down serial interface
- Total resistance: 10 kΩ, 50 kΩ, 100 kΩ
- SOIC, TSSOP, MSOP and TDFN packages

APPLICATIONS

- Auto calibration
- Remote control adjustment
- Offset, gain and zero controls
- Rewritable calibration
- Contrast, brightness and volume controls
- Motor-controlled, feedback system
- Programmable analog function

DP 7114
DIGITAL POTENTIOMETERS

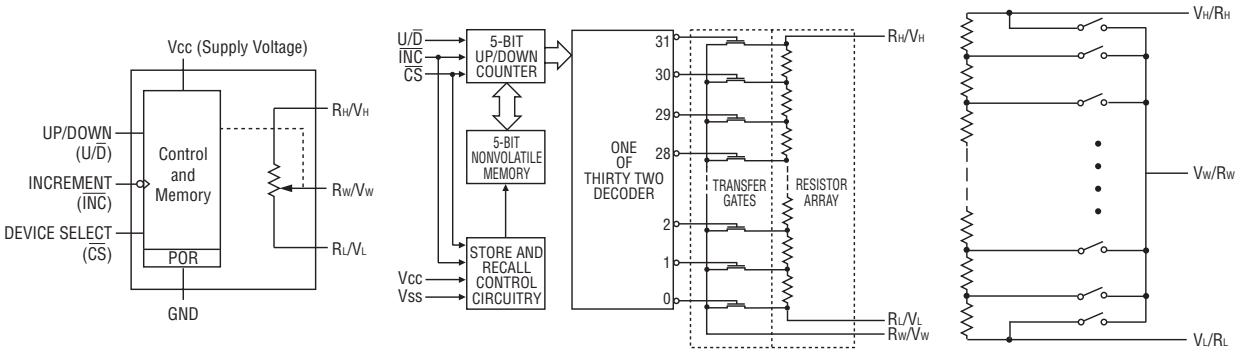
SUMMARY

The DP7114 is a programmable digital potentiometer designed to replace mechanical potentiometers and variable resistors. Automated adjustment by product automation line is ideal. The DP7114 makes this possible and is suitable for applications where it is difficult to operate when machines require constant adjustment or in case of danger or at remote locations.

The DP7114 has a 32-tap resistance array between two terminals, RH and RL. The up/down counter and decoder controlled by 3 input terminals determines the tap connected to wiper resistance RW. Wiper settings stored in nonvolatile memory can not be lost even at power shutoff and will be automatically restored when power returns. Not affected by stored settings, the wiper can test new setting of the system.

The wiper control of the DP7114 is made by three input terminals, $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$. The $\overline{INC}$ input increments wiper to direction determined in U/$\overline{D}$ input logic condition. The $\overline{CS}$ input terminal is for device-select use and used when wiper position is stored before power shutoff. The digital potentiometer can be used as a voltage partial pressure device or 2-terminal variable resistor. The DP7114 offers valuable capabilities and programmability to a wide variety of applications such as parameter adjustment and signal processing.

CONFIGURATION

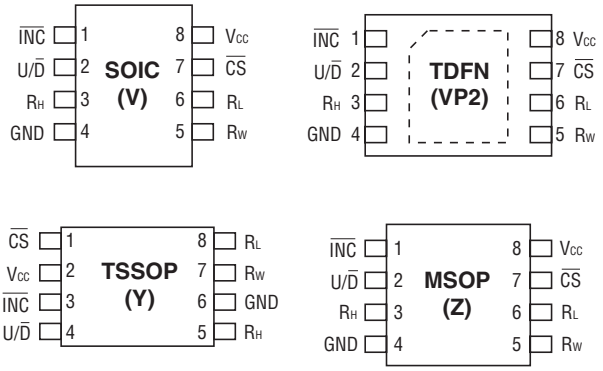


Circuit block diagram

Electricity-equivalent circuit of POT section

DP 7114
DIGITAL POTENTIOMETERS

CONTACT LAYOUT



TERMINAL FUNCTIONS

Terminal name	Functions
$\overline{INC}$	Increment control input
U/$\overline{D}$	Up/Down control input
R_H	High-end potentiometer terminal
GND	Ground
R_W	Wiper terminal
R_L	Low-end potentiometer terminal
$\overline{CS}$	Chip select
V_{CC}	Power voltage

FUNCTIONS OF EACH TERMINAL

$\overline{INC}$: Increment control input
This $\overline{INC}$ input moves wiper to the up and down direction selected by conditions of U/$\overline{D}$ input at the VIL edge.

U/$\overline{D}$: Up/down control input
U/$\overline{D}$ input controls moving direction of wiper. When U/$\overline{D}$ is in H state and $\overline{CS}$ is in L state, this input moves the wiper to R_H from transition state of H - L of the INC. When U/$\overline{D}$ and $\overline{CS}$ are in L state, it moves the wiper to R_L direction in the transition of H to L of the $\overline{INC}$.

R_H: High-end potentiometer terminal
R_H is a high-end potentiometer terminal. This terminal does not require higher voltage than R_L terminal. But, R_H voltage should not be over V_{CC} nor under GND.

R_W: Wiper terminal
R_W is a wiper terminal of potentiometer. The position within resistance arrays are controlled by control input terminals of $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$.

IR$_L$: Low-end potentiometer terminal
R_L is a low-end potentiometer terminal. This terminal does not need to connect lower voltage than R_H terminal. But, R_L voltage should not be over V_{CC} nor under GND. R_H and R_L can be changed electrically.

$\overline{CS}$: Chip select
Chip select input is used to make a DP7114 control input effective and becomes effective in the L state. When $\overline{CS}$ is in the H state, inputs of $\overline{INC}$ and U/$\overline{D}$ does not give effect or change to wiper position.

DP 7114
DIGITAL POTENTIOMETERS

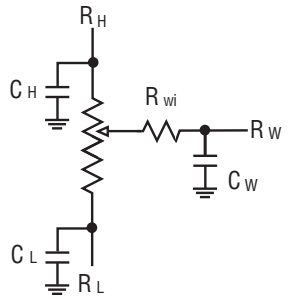
OPERATION EXPLANATION

The R_H and R_L terminals of the DP7114 are equivalent to high and low terminals of mechanical potentiometers. The DP7114 is a digital potentiometer of which R_W terminal operates as a wiper. The model has 32 taps including terminators of R_H and R_L. There are 31 resistance arrays linearly connected between terminal R_H and R_L. This wiper terminal is connected to one of 32 taps and controlled by 3 inputs of $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. This input controls the 5-bit up/down counter which can decode to select wiper position. Selected wiper position data is stored into nonvolatile memories by $\overline{INC}$ and $\overline{CS}$ inputs.

When $\overline{CS}$ is in the L state, DP7114 is selected and responds to U/$\overline{D}$ and $\overline{INC}$ inputs. In transition from H of $\overline{INC}$ to L, wiper will be incremented or decremented. The wipe acts like mechanical and does not move from the last position. Counter values will be saved in nonvolatile memories by transition from H of the $\overline{INC}$ input to H of the $\overline{CS}$. When DP7114 power is shut down, counter position saved in the last will be kept in nonvolatile memories. When DP7114 power returns, contents within memories will be renewed and counter values are set on the counter. When $\overline{INC}$ is in L state, DP7114 will not be selected and shut down without saving the current wiper position in nonvolatile memories, thereby the system will recall preset values always stored in nonvolatile memories.

OPERATION MODE

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



Equivalent circuit of potentiometer

DP 7114
DIGITAL POTENTIOMETERS

■ ABSOLUTE MAXIMUM RATINGS

Supply voltage
- V_{CC} to GND ・・・・・・・・・・・・・・・・・・・・ −0.5 V ～ +7 V

Inputs
- $\overline{CS}$ to GND ・・・・・・・・・・・・・・・・・ −0.5 V ～ Vcc + 0.5 V
- $\overline{INC}$ to GND ・・・・・・・・・・・・・・・・・ −0.5 V ～ Vcc + 0.5 V
- U/$\overline{D}$ to GND ・・・・・・・・・・・・・・・・・ −0.5 V ～ Vcc + 0.5 V
- R_H to GND ・・・・・・・・・・・・・・・・・・・・ −0.5 V ～ Vcc + 0.5 V
- R_L to GND ・・・・・・・・・・・・・・・・・・・・ −0.5 V ～ Vcc + 0.5 V
- R_W to GND ・・・・・・・・・・・・・・・・・・・・ −0.5 V ～ Vcc + 0.5 V

Operating ambient temperature
- Industrial（'I' suffix）・・・・・・・・・・・・・・・・ −40 °C ～ +85 °C
- ジJunction Temperature ・・・・・・・・・・・・・・・・・・ +150 °C
- Storage Temperature ・・・・・・・・・・・・・・・ −65 °C ～ +150 °C
- Lead Soldering（10 sec max）・・・・・・・・・・・・・・・ +300 °C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

■ RELIABILITY CHARACTRISTICS

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
V_{ZAP}(1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000	—	—	Volts
I_{LTH}(1)(2)	Latch-Up	JEDEC Standard 17	100	—	—	mA
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	100	—	—	Years
N_{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000	—	—	Stores

* Typ. = Typical

■ DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the specs are defined at
Vcc = +2.5 V to +6.0 V.

● Power supply

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
V_{CC}	Operating Voltage Range	—	2.5	—	6.0	V
I_{CC1}	Supply Current (Increment) Supply Current (Increment)	V_{CC} = 6 V, f = 1 MHz, I_W = 0 V_{CC} = 6 V, f = 250 kHz, I_W = 0	— —	— —	100 50	µA
I_{CC2}	Supply Current (Write) Supply Current (Write)	Programming, V_{CC} = 6 V V_{CC} = 3 V	— —	— —	1 500	mA µA
I_{SB1}(2)	Supply Current (Standby)	$\overline{CS}$ = Vcc − 0.3 V U/$\overline{D}$, $\overline{INC}$ = Vcc − 0.3 V or GND	— —	— —	1	µA

* Typ. = Typical

● Logic inputs

Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0 V	—	—	−10	µA
V_{IH2}	CMOS High Level input Voltage	2.5 V ≦ V_{CC} ≦ 6 V	Vcc × 0.7	—	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level input Voltage		−0.3	—	V_{CC} × 0.2	V

* Typ. = Typical

Notes : 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1 V to Vcc +1 V.
3. Iw = source or sink current.
4. The value is for reference.

DP 7114
DIGITAL POTENTIOMETERS

■ POTENTIOMETER PARAMETERS

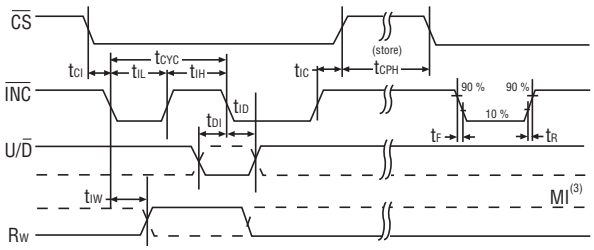
Symbol	Parameter	Conditions	Min.	Typ.*	Max.	Units
R_{POT}	Potentiometer Resistance	–10 Device	—	10	—	kΩ
		–50 Device	—	50	—	
		–00 Device	—	100	—	
R_{TOL}	Pot Resistance Tolerance	—	—	—	±20	%
V_{RH}	Voltage on R_H pin	—	0	—	V_{CC}	V
V_{RL}	Voltage on R_L pin	—	0	—	V_{CC}	V
RES	Resolution	—	—	3.2	—	%
INL	Integral Linearity Error	—	—	—	0.5	LSB
DNL	Differential Linearity Error	—	—	—	0.25	LSB
R_{WI}	Wiper Resistance	V_{CC} = 5 V, I_W = 1 mA	—	70	200	Ω
		V_{CC} = 2.5 V, I_W = 1 mA	—	150	400	Ω
I_{WI}	Wiper Current	—	– 4.4	—	4.4	mA
TC_{RPOT}	TC of Pot Resistance	—	—	300	—	ppm/°C
TC_{RATIO}	Ratiometric TC	—	—	—	20	ppm/°C
V_N	Noise	100 kHz / 1 kHz	—	8/24	—	nV/√Hz
$C_H/C_L/C_W$	Potentiometer Capacitances	—	—	8/8/25	—	pF
fc	Frequency Response	Passive Attenuator, 10 kΩ	—	1.7	—	MHz

* Typ. = Typical

■ AC TEST CONDITIONS

V_{CC} Range	2.5 V ≦ Vcc ≦ 6 V
Input Pulse Levels	0.2 V_{CC} to 0.7 V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V_{CC}

■ AC TIMING DIAGRAM



■ AC ELECTRICAL CHARACTERISTICS

Vcc = +2.5 V to +6.0 V, V_H = Vcc, V_L = 0 V

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100	—	—	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	—	—	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	—	—	ns
t_{IL}	$\overline{INC}$ LOW Period	250	—	—	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	—	—	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	—	—	µs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	—	—	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	—	—	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	—	1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	1	—	—	µs
t_R, t_F(2)	$\overline{INC}$ Input Rise and Fall Time	—	—	500	µs
t_{PU}(2)	Power-up to Wiper Stable	—	—	1	ms
t_{WR}	Store Cycle	—	5	10	ms

(1) The value is measured at temperature 25 °C and at the above defined power supply voltage. (Typ. = Typical)

Notes: 1. The value is for reference.
2. MI shows minimum change unit of wiper output by changing wiper position.

DP series
DIGITAL POTENTIOMETERS

■ PART NUMBER DESIGNATION

DP7xxx X X –xx –x Tx

Product number

Package

Green package
SD : SC70 Z : MSOP
TB : SOT-23 V※1 : SOIC
VP2 : TDFN Y : TSSOP

Temperature range

I : – 40 °C ~ 85 °C

Resistance value

01 : 1 kΩ 25 : 2.5 kΩ 10 : 10 kΩ 50 : 50 kΩ 00 : 100 kΩ

Form of packaging

T 1 : Taping (1,000 pcs./reel)
T 2 : Taping (2,000 pcs./reel)
T 3 : Taping (3,000 pcs./reel)

Lead finish

Blank : Matte-Tin
G : NiPdAu※3 NiPdAu※3

※1 : The relevant products are as follows.
DP7111/DP7112/DP7113/DP7114/DP7115

※2 : The relevant products are actollows.
DP7110 / DP7111 / DP7112 / DP7113 /
DP7114 / DP7115 / DP7118 / DP7119 /
DP7120 / DP7121 / DP7122 / DP7132 /
DP7140 / DP7172
Except MSOP package of DP7111, DP7113

● Taping code and quantity

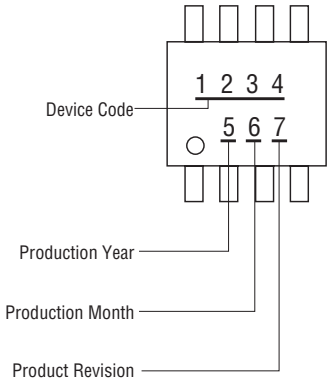
Package	Pin no.	Taping quantity (pcs./reel)		
		1,000	2,000	3,000
SC70	5/6			○
SOT-23	5/6/8			○
TDFN	8			○
MSOP	8			○
MSOP	10			○
SOIC	8			○
TSSOP	8			○
TSSOP	20		○	
TSSOP	24		○	

DP series
DIGITAL POTENTIOMETERS

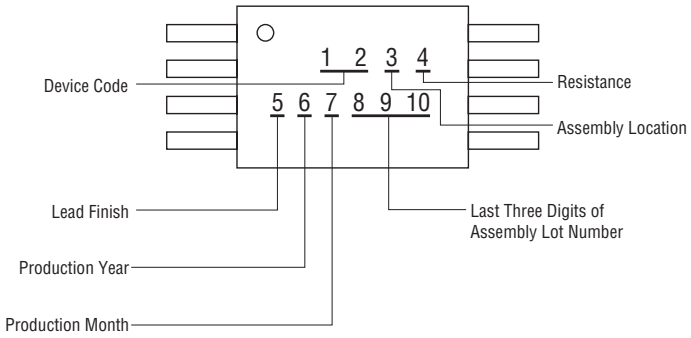
■ MARKING

Marking condition of IC top view is as follows;

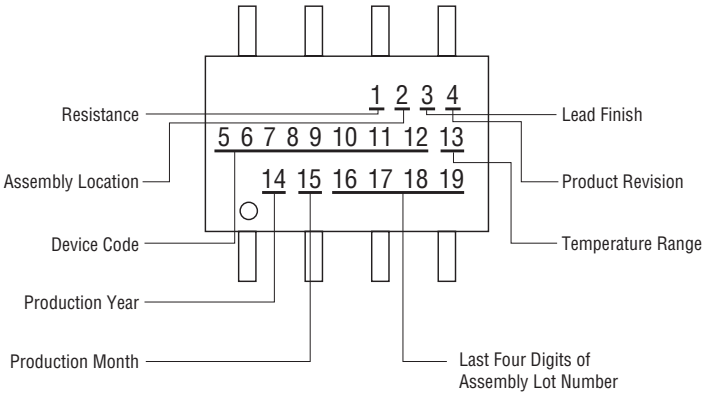
● MSOP



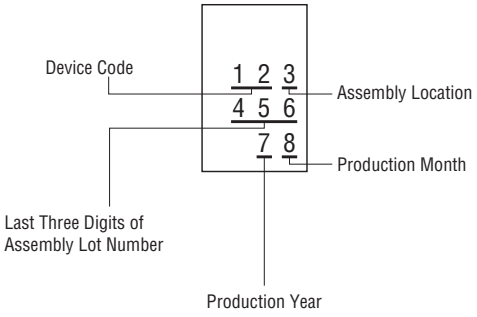
● TSSOP



● SOIC

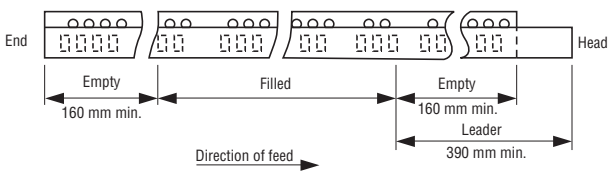


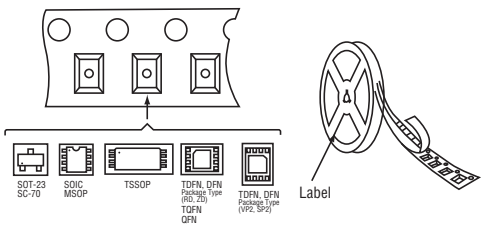
● TDFN



※ Regarding the details of each part number, please refer to respective specifications.

■ TAPING PACKAGING SPECIFICATIONS





DP series
DIGITAL POTENTIOMETERS

■ Application Notes and Design Notes

Application Notes (AN) and Design Notes (DN) are available as follows.
Please request these notes from one of our sales offices.

No.	Title
AN7	Programmable Analog Functions
AN8	Everything You wanted to know About Digital Potentiometers
AN9	Minimizing the Temperature Dependence of Digital Potentiometers
DN1	Push-Button Control of Digital Potentiometers with an increment/decrement interface
DN2	Electronics versus Mechanical Potentiometers-A Comparison
DN3	Operating speed of Digital Potentiometers
DN4	Improving the Resolution of Digital Potentiometers Applications
DN5	Making a Stop-less Digital Potentiometers
DN6	Power-Up and Power-Down characteristics for Digital Potentiometers

■ DEVELOPMENT SUPPORT KIT FOR DP

DP control can be carried out using a special interface board.
With this, your product development time can be shortened.

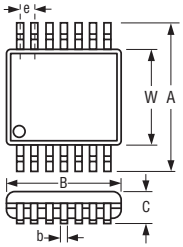
- OS : Windows98/2000/XP
- I/O : USB interface
- Software : Copal DP

※ : Please order from one of our sales offices

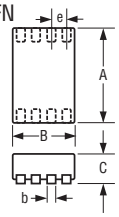
■ OUTLINE DIMENSIONS

Unit : mm

SC70/SOT-23/MSOP/
SOIC/TSSOP



TDFN



● SC70/SOT-23/MSOP/SOIC/TSSOP/TDFN

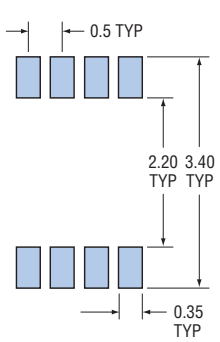
mm

Packaging	Pin	A(Max./Min.)	B(Max./Min.)	W(Max./Min.)	C(Max./Min.)	b(Max./Min.)	e
SC70	5/6	2.40/1.80	2.20/1.80	1.35/1.15	1.10/0.80	0.30/0.15	0.65
SOT-23	5/6	2.80(Typ)	2.90(Typ)	1.60(Typ)	1.45/0.90	0.50/0.30	0.95
SOT-23	8	2.80(Typ)	2.90(Typ)	1.60(Typ)	1.45/0.90	0.38/0.28	0.65
TDFN	8	3.10/2.90	2.10/1.90	——	0.80/0.70	0.30/0.20	0.50
MSOP	8	5.00/4.80	3.10/2.90	3.10/2.90	0.95/0.75	0.38/0.22	0.65
MSOP	10	5.05/4.75	3.10/2.90	3.10/2.90	1.1max	0.27/0.17	0.50
SOIC	8	6.20/5.80	5.0/4.80	4.00/3.80	1.75/1.35	0.51/0.33	1.27
TSSOP	8	6.50/6.30	3.10/2.90	4.50/4.30	1.2max	0.30/0.19	0.65
TSSOP	20	6.50/6.30	6.60/6.40	4.50/4.30	1.2max	0.30/0.19	0.65
TSSOP	24	6.55/6.25	7.90/7.70	4.50/4.30	1.2max	0.30/0.19	0.65

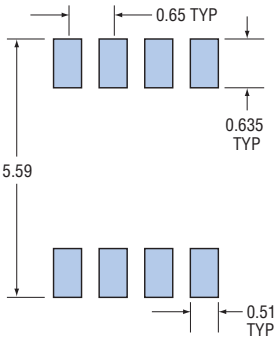
■ RECOMMENDED P. C. B. PAD OUTLINE DIMENSIONS

Unit: mm

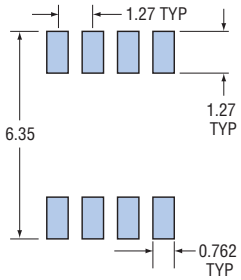
● 8 pins TDFN



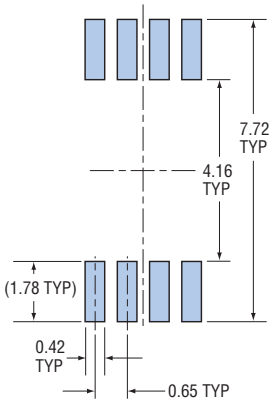
● 8 pins MSOP



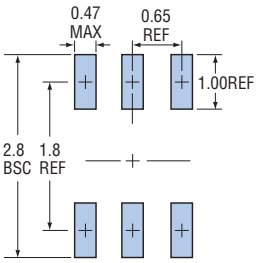
● 8 pins SOIC



● 8 pinsTSSOP



● 6 pins SC70



HANDLING NOTES
DIGITAL POTENTIOMETERS

■ PRECAUTIONS WHEN USING

● Processing of up/down control $\overline{CS}$ and $\overline{INC}$ pins

When power is turned ON/OFF, please use a fixed resistor to pull $\overline{CS}$ and $\overline{INC}$ pins up to Vcc in order to set them HIGH. This is because the $\overline{CS}$ pin and $\overline{INC}$ pin are connected by the NOR circuit, and DP operating mode is set by these signals. If the $\overline{CS}$ signal is LOW when power is turned ON/OFF, signal receiving status results, and unintended wiper tap movement may occur due to the $\overline{INC}$ and U/D signals, so the $\overline{CS}$ pin should always be HIGH. Further, $\overline{CS}$ and $\overline{INC}$ pins should be pulled up to Vcc and set HIGH in order to prevent unintended write operation during power start-up transition.

● Restart of power supply (Vcc)

1. Drop power supply voltage to 0V when power is down. For power cut-off, power supply voltage must be set to less than 0.1 V in order to ensure correct operation of the memory read-out POR (power on recall) circuit the next time power is turned on.
2. Please wait about 1 second before power-up again in order to have enough time to reset for internal circuit.

● Sequence for Digital Power Supply Vcc and Analog Pin Voltage

When applying voltage to the analog pins (Vh, Vw, Vl), please input simultaneously with digital voltage (Vcc) or after steady state is reached. This is because the analog pins (Vh, V2, Vl) have parasitic diodes formed between Vcc and Vss by the process.

This means that when the power supply sequence is not correct, the parasitic diode is forward biased, giving rise to the possibility of misoperation or even damage resulting from excess current, or affecting the data read-out function (POR) from memory during power-up. Therefore, sufficient attention must be paid to power supply sequence design.