

Bias Resistor Transistor

NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

● Applications

Inverter, Interface, Driver

● Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making the device design easy.

- We declare that the material of product compliance with RoHS requirements.

- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V _{CB0}	50	V
Collector-emitter voltage	V _{CE0}	50	V
Emitter-base voltage	V _{EB0}	5	
Collector current	I _c	100	mA
Collector power dissipation	P _c	200	mW
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

DEVICE MARKING AND RESISTOR VALUES

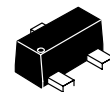
Device	Marking	R1 (K)	R2 (K)	Shipping
LDTTC144TET1G S-LDTTC144TET1G	H5	47	-	3000/Tape & Reel
LDTTC144TET3G S-LDTTC144TET3G	H5	47	-	10000/Tape & Reel

● Electrical characteristics (Ta=25°C)

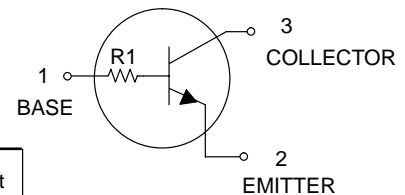
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV _{CB0}	50	-	-	V	I _c =10μA
Collector-emitter breakdown voltage	BV _{CE0}	50	-	-	V	I _c =2.0mA
Emitter-base breakdown voltage	BV _{EB0}	5	-	-	V	I _E =50μA
Collector cutoff current	I _{CB0}	-	-	0.5	μA	V _{CB} =50V
Emitter cutoff current	I _{EB0}	-	-	0.5	μA	V _{EB} =4V
Collector-emitter saturation voltage	V _{CE(sat)}	-	-	0.3	V	I _c /I _B =5mA/0.5mA
DC current transfer ratio	h _{FE}	100	250	600	-	V _{CE} =5V, I _c =1mA
Input resistance	R _i	32.9	47	61.1	kΩ	-
Transition frequency	f _T *	-	250	-	MHz	V _{CE} =10V, I _E =-5mA, f=100MHz

Characteristics of built-in transistor

LDTTC144TET1G
S-LDTTC144TET1G



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LDTC144TET1G;S-LDTC144TET1G

● **Electrical characteristic curves**

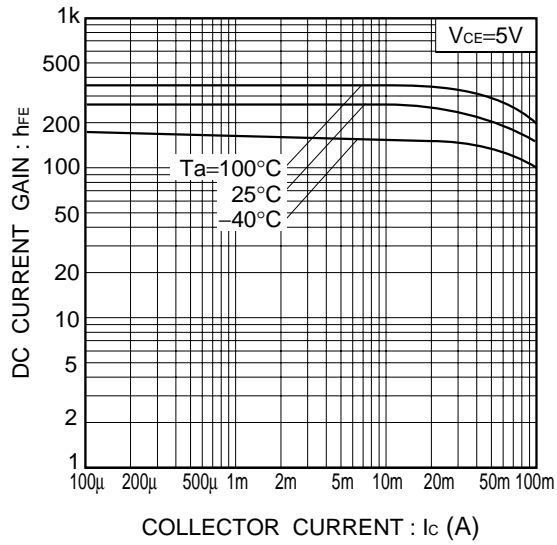


Fig.1 DC current gain vs. collector current

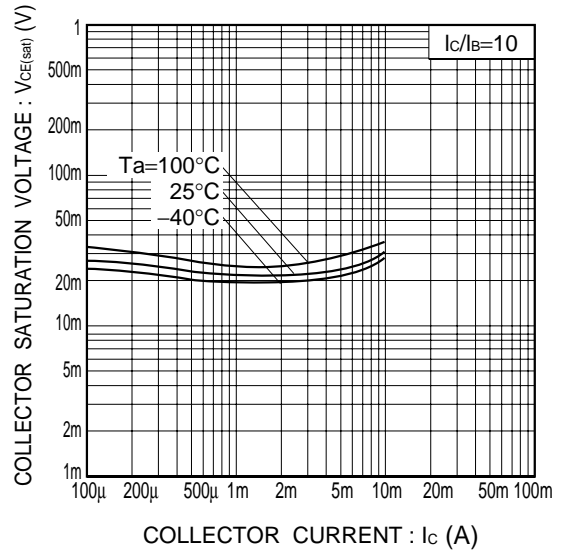
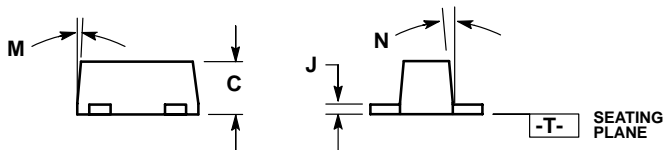
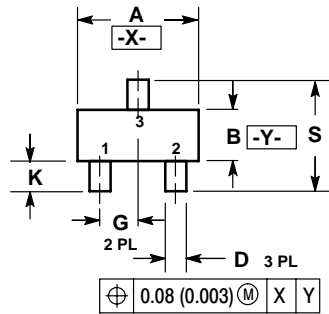


Fig.2 Collector-emitter saturation voltage vs. collector current

LDTC144TET1G;S-LDTC144TET1G

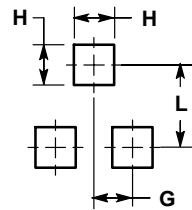
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



RECOMMENDED PATTERN OF SOLDER PADS