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ON Semiconductor®

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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

December 2010

NC7SV57 / NC7SV58 TinyLogic® ULP-A Universal Configurable Two-Input Logic Gates

Features

- 0.9V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at V_{CC} from 0.9V to 3.6V
- Extremely High Speed t_{PD}
  - 2.5ns: Typical for 2.7V to 3.6V V_{CC}
  - 3.1ns: Typical for 2.3V to 2.7V V_{CC}
  - 4.0ns: Typical for 1.65V to 1.95V V_{CC}
  - 6.0ns: Typical for 1.4V to 1.6V V_{CC}
  - 8.0ns: Typical for 1.1V to 1.3V V_{CC}
  - 23.0ns: Typical for 0.9V V_{CC}
- Power-Off High-Impedance Inputs and Outputs
- High Static Drive (I_{OH}/I_{OL})
  - ±24mA at 3.00V V_{CC}
  - ±18mA at 2.30V V_{CC}
  - ±6mA at 1.65V V_{CC}
  - ±4mA at 1.4V V_{CC}
  - ±2mA at 1.1V V_{CC}
  - ±0.1mA at 0.9V V_{CC}
- Proprietary Quiet Series™ Noise/EMI Reduction
- Ultra-Small MicroPak™ Package
- Ultra-Low Dynamic Power

Description

The NC7SV57 and NC7SV58 are universal configurable two-input logic gates from Fairchild's Ultra-Low Power (ULP-A) series of TinyLogic®. ULP-A is ideal for applications that require extreme high-speed, high drive, and low power. This product is designed for a wide low-voltage operating range (0.9V to 3.6V V_{CC}) and applications that require more drive and speed than the TinyLogic® ULP series, but still offer best-in-class, low-power operation.

Each device is capable of being configured for 1 of 5 unique two-input logic functions. Any possible two-input combinatorial logic function can be implemented, as shown in the *Function Selection Table*. Device functionality is selected by how the device is wired at the board level. *Figures 1 through 10* illustrate how to connect the NC7SV57 and NC7SV58, respectively, for the desired logic function. All inputs have been implemented with hysteresis.

The NC7SV57 and NC7SV58 are uniquely designed for optimized power and speed and are fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SV57P6X	V57	6-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SV57L6X	H3	6-Lead Micropak™, 1.0mm Wide	5000 Units on Tape & Reel
NC7SV57FHX	H3	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	
NC7SV58P6X	V58	6-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SV58L6X	H4	6-Lead Micropak™, 1.0mm Wide	5000 Units on Tape & Reel
NC7SV58FHX	H4	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	

Battery Life

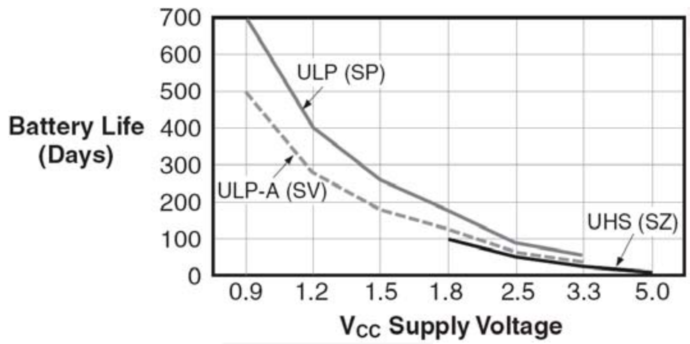


Figure 1. Battery Life vs. V_{CC} Supply Voltage

Notes:

1. TinyLogic® ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.
   Battery Life = ($V_{battery}$•$I_{battery}$•.9)/(P_{device})/24hrs/day
   where P_{device} = (I_{CC} • V_{CC}) + (C_{PD} + C_L) • V_{CC}^2 • f.
2. Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L = 15pF load.

Pin Configurations

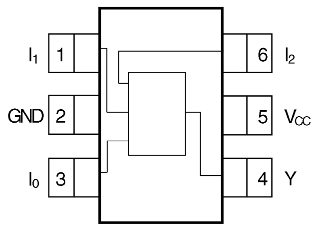


Figure 2. SC70 (Top View)

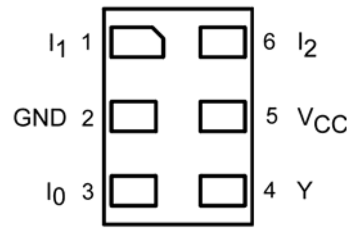


Figure 3. MicroPak™ (Top Through View)

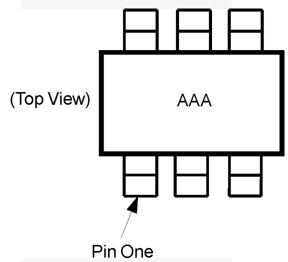


Figure 4. Pin 1 Orientation

Notes:

3. AAA represents product code top mark (*see Ordering Information*).
4. Orientation of top mark determines pin one location.
5. Reading the top mark left to right, pin one is the lower left pin.

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	I_1	Data Input
2	2	GND	Ground
3	3	I_0	Data Input
4	4	Y	Output
5	5	V_{CC}	Supply Voltage
6	6	I_2	Data Input

Function Table

Inputs			NC7SV57	NC7SV58
I_2	I_1	I_0	$Y = \overline{(I_0)} \bullet \overline{(I_2)} + (I_1) \bullet (I_2)$	$Y = (I_0) \bullet \overline{(I_2)} + \overline{(I_1)} \bullet (I_2)$
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	L	H
H	H	L	H	L
H	H	H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Function Selection Table

2-Input Logic Function	Device Selection	Connection Configuration
2-Input AND	NC7SV57	Figure 5
2-Input AND with Inverted Input	NC7SV58	Figure 11, Figure 12
2-Input AND with Both Inputs Inverted	NC7SV57	Figure 8
2-Input NAND	NC7SV58	Figure 10
2-Input NAND with Inverted Input	NC7SV57	Figure 6, Figure 7
2-Input NAND with Both Inputs Inverted	NC7SV58	Figure 13
2-Input OR	NC7SV58	Figure 13
2-Input OR with Inverted Input	NC7SV57	Figure 6, Figure 7
2-Input OR with Both Inputs Inverted	NC7SV58	Figure 10
2-Input NOR	NC7SV57	Figure 8
2-Input NOR with Inverted Input	NC7SV58	Figure 10, Figure 11
2-Input NOR with Both Inputs Inverted	NC7SV57	Figure 5
2-Input XOR	NC7SV58	Figure 14
2-Input XNOR	NC7SV57	Figure 9

NC7SV57 Logic Configurations

Figure 5 through Figure 9 show the logical functions that can be implemented using the NC7SV57. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical implementation is next to the board-level physical implementation of how the pins of the function should be connected.

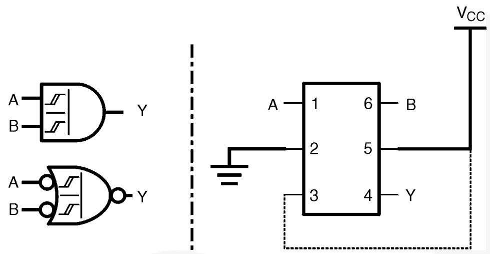


Figure 5. 2-Input AND Gate

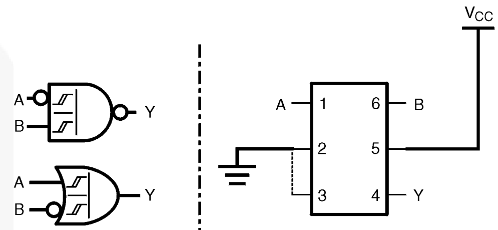


Figure 6. 2-Input NAND Gate with Inverted A Input

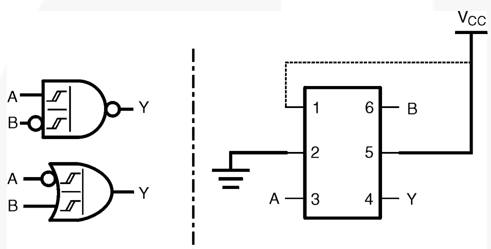


Figure 7. 2-Input NAND with Inverted B Input

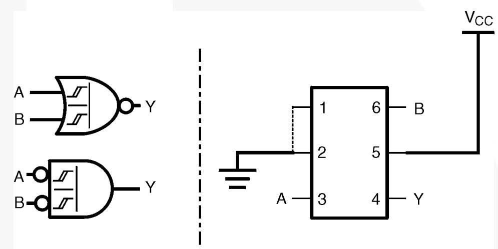


Figure 8. 2-Input NOR Gate

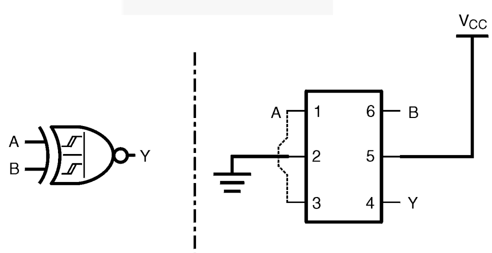


Figure 9. 2-Input XNOR Gate

NC7SV58 Logic Configurations

Figure 10 through Figure 14 show the logical functions that can be implemented using the NC7SV58. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical implementation is next to the board-level physical implementation of how the pins of the function should be connected.

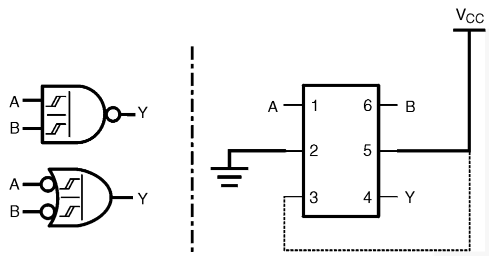


Figure 10. 2-Input NAND Gate

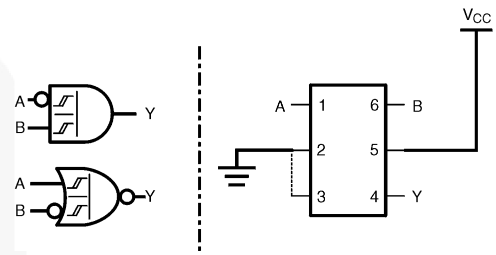


Figure 11. 2-Input AND Gate with Inverted A Input

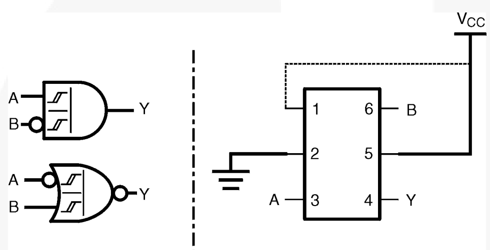


Figure 12. 2-Input AND with Inverted B Input

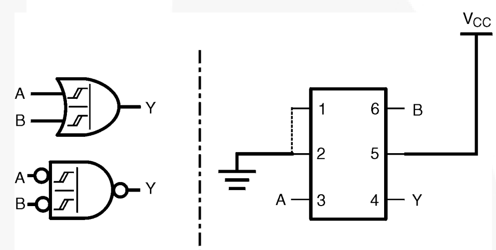


Figure 13. 2-Input OR Gate

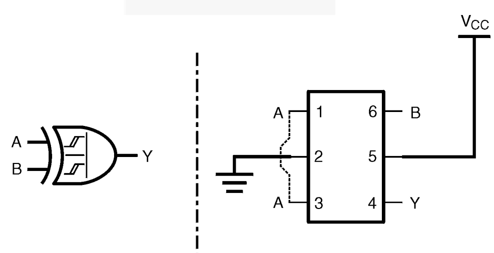


Figure 14. 2-Input XOR Gate

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	4.6	V
V_{IN}	DC Input Voltage		-0.5	4.6	V
V_{OUT}	DC Output Voltage	HIGH or LOW State[6]	-0.5	V_{CC} + 0.5	V
		V_{CC}=0V	-0.5	4.6	
I_{IK}	DC Input Diode Current	V_{IN} < 0V		±50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0V		-50	mA
		V_{OUT} > V_{CC}		+50	
I_{OH} / I_{OL}	DC Output Source / Sink Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
P_D	Power Dissipation at +85°C	MicroPak™-6		130	mW
		SC70-6		150	
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charged Device Model, JEDEC:JESD22-C101			2000	

Note:
6. IO absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		0.9	3.6	V
V_{IN}	Input Voltage		0	3.6	V
V_{OUT}	Output Voltage	V_{CC}=0V	0	3.6	V
		HIGH or LOW State	0	V_{CC}	
I_{OH}/I_{OL}	Output Current	V_{CC}=3.0V to 3.6V		±24.0	mA
		V_{CC}=2.3V to 2.7V		±18.0	
		V_{CC}=1.65V to 1.95V		±6.0	
		V_{CC}=1.4V to 1.6V		±4.0	
		V_{CC}=1.1V to 1.3V		±2.0	
		V_{CC}=0.9V		±0.1	μA
T_A	Operating Temperature, Free Air		-40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate	V_{IN}=0.8V to 2.0, V_{CC}=3.0V		10	ns/V
θ_{JA}	Thermal Resistance	SC70-6		425	°C/W
		MicroPak™-6		500	
		MicroPak2™-6		560	

Note:
7. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C		T_A=-40 to 85°C		Units
				Min.	Max.	Min.	Max.	
V_P	Positive Threshold Voltage	0.90		0.30	0.70	0.30	0.70	V
		1.10		0.40	1.00	0.40	1.00	
		1.40		0.50	1.40	0.50	1.40	
		1.65		0.70	1.50	0.70	1.50	
		2.30		1.00	1.80	1.00	1.80	
		2.70		1.30	2.20	1.30	2.20	
V_N	Negative Threshold Voltage	0.90		0.10	0.60	0.10	0.60	V
		1.10		0.15	0.70	0.15	0.70	
		1.40		0.20	0.80	0.20	0.80	
		1.65		0.25	0.90	0.25	0.90	
		2.30		0.40	1.15	0.40	1.15	
		2.70		0.60	1.50	0.60	1.50	
V_H	Hysteresis Voltage	0.90		0.07	0.50	0.07	0.50	V
		1.10		0.08	0.60	0.08	0.60	
		1.40		0.10	0.80	0.10	0.80	
		1.65		0.15	1.00	0.15	1.00	
		2.30		0.25	1.10	0.25	1.10	
		2.70		0.40	1.20	0.40	1.20	
V_{OH}	HIGH Level Output Voltage	0.90	I_{OH}=-100µA	V_{CC}-0.1		V_{CC}-0.1		V
		$1.10 \le V_{CC} \le 1.30$		V_{CC}-0.1		V_{CC}-0.1		
		$1.40 \le V_{CC} \le 1.60$		V_{CC}-0.2		V_{CC}-0.2		
		$1.65 \le V_{CC} \le 1.95$		V_{CC}-0.2		V_{CC}-0.2		
		$2.30 \le V_{CC} \le 2.70$		V_{CC}-0.2		V_{CC}-0.2		
		$2.70 \le V_{CC} \le 3.60$		V_{CC}-0.2		V_{CC}-0.2		
		$1.10 \le V_{CC} \le 1.30$	I_{OH}=-2mA	.75 x V_{CC}		.75 x V_{CC}		
		$1.40 \le V_{CC} \le 1.60$	I_{OH}=-4mA	.75 x V_{CC}		.75 x V_{CC}		
		$1.65 \le V_{CC} \le 1.95$	I_{OH}=-6mA	1.25		1.25		
		$2.30 \le V_{CC} \le 2.70$		2.0		2.0		
		$2.30 \le V_{CC} \le 2.70$	I_{OH}=-12mA	1.8		1.8		
		$2.70 \le V_{CC} \le 3.60$		2.2		2.2		
		$2.30 \le V_{CC} \le 2.70$	I_{OH}=-18mA	1.7		1.7		
		$2.70 \le V_{CC} \le 3.60$		2.4		2.4		
		$2.70 \le V_{CC} \le 3.60$	I_{OH}=-24mA	2.2		2.2		

Continued on following page….

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C		T_A=-40 to 85°C		Units
				Min.	Max.	Min.	Max.	
V_{OL}	LOW Level Output Voltage	0.90	I_{OL}=100µA		0.1		0.1	V
		$1.10 \le V_{CC} \le 1.30$			0.1		0.1	
		$1.40 \le V_{CC} \le 1.60$			0.2		0.2	
		$1.65 \le V_{CC} \le 1.95$			0.2		0.2	
		$2.30 \le V_{CC} \le 2.70$			0.2		0.2	
		$2.70 \le V_{CC} \le 3.60$			0.2		0.2	
		$1.10 \le V_{CC} \le 1.30$	I_{OL}=2mA		.25 x V_{CC}		.25 x V_{CC}	
		$1.40 \le V_{CC} \le 1.60$	I_{OL}=4mA		.25 x V_{CC}		.25 x V_{CC}	
		$1.65 \le V_{CC} \le 1.95$	I_{OL}=6mA		0.3		0.3	
		$2.30 \le V_{CC} \le 2.70$	I_{OL}=12mA		0.4		0.4	
		$2.70 \le V_{CC} \le 3.60$			0.4		0.4	
		$2.30 \le V_{CC} \le 2.70$	I_{OL}=18mA		0.6		0.6	
		$2.70 \le V_{CC} \le 3.60$			0.4		0.4	
		$2.70 \le V_{CC} \le 3.60$	I_{OL}=24mA		0.55		0.55	
I_{IN}	Input Leakage Current	0.90 to 3.60	$0 \le V_{IN} \le 3.6V$		±0.1		±0.5	µA
I_{OFF}	Power Off Leakage Current	0	$0 \le (V_{IN}, V_O) \le 3.60$		0.5		0.5	µA
I_{CC}	Quiescent Supply Current	0.90 to 3.60	$V_{IN}=V_{CC}$ or GND		0.9		0.9	µA
			$V_{CC} \le V_{IN} \le 3.6V$				±0.9	

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to 85°C		Units	Figure
				Min.	Typ.	Min.	Typ.	Min.		
t_{PHL}, t_{PLH}	Propagation Delay	0.90	C_L=15pF, R_L=1MΩ		15.0				ns	Figure 15 Figure 16
		$1.10 \le V_{CC} \le 1.30$	C_L=15pF, R_L=2KΩ	4.0	8.0	16.5	3.3	31.0		
		$1.40 \le V_{CC} \le 1.60$		2.0	6.0	10.0	2.0	12.0		
		$1.65 \le V_{CC} \le 1.95$	C_L=30pF, R_L=500Ω	2.0	4.0	9.1	1.9	10.0		
		$2.30 \le V_{CC} \le 2.70$		1.5	3.1	6.2	1.4	6.7		
		$2.70 \le V_{CC} \le 3.60$		1.2	2.5	5.4	1.2	6.1		
C_{IN}	Input Capacitance	0			8				pF	
C_{OUT}	Output Capacitance	0			12				pF	
C_{PD}	Power Dissipation Capacitance	0.90 to 3.60	V_I=0V or V_{CC}, f=10MHz		10				pF	

AC Loadings and Waveforms

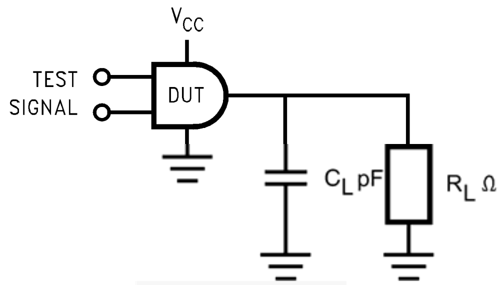


Figure 15. AC Test Circuit

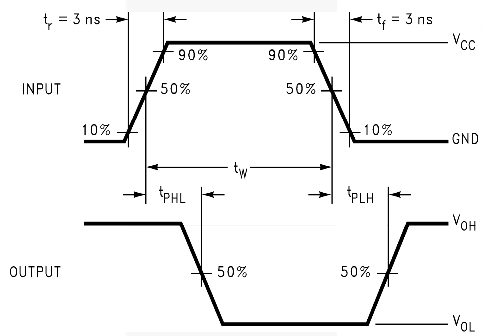


Figure 16. AC Waveforms

Symbol	V_{CC}					
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**	**1.5V ± 0.10V**	**1.2V ± 0.10V**	**0.9V**
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$

Physical Dimensions

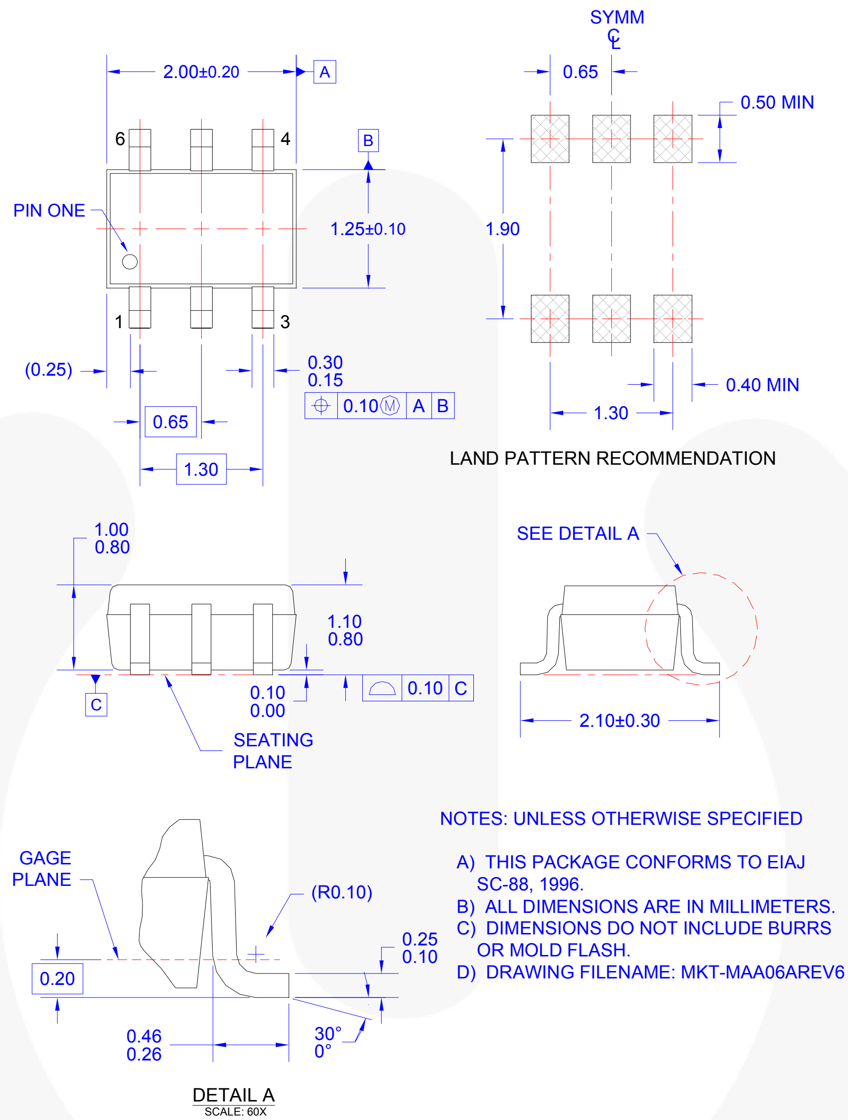


Figure 17. 6-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

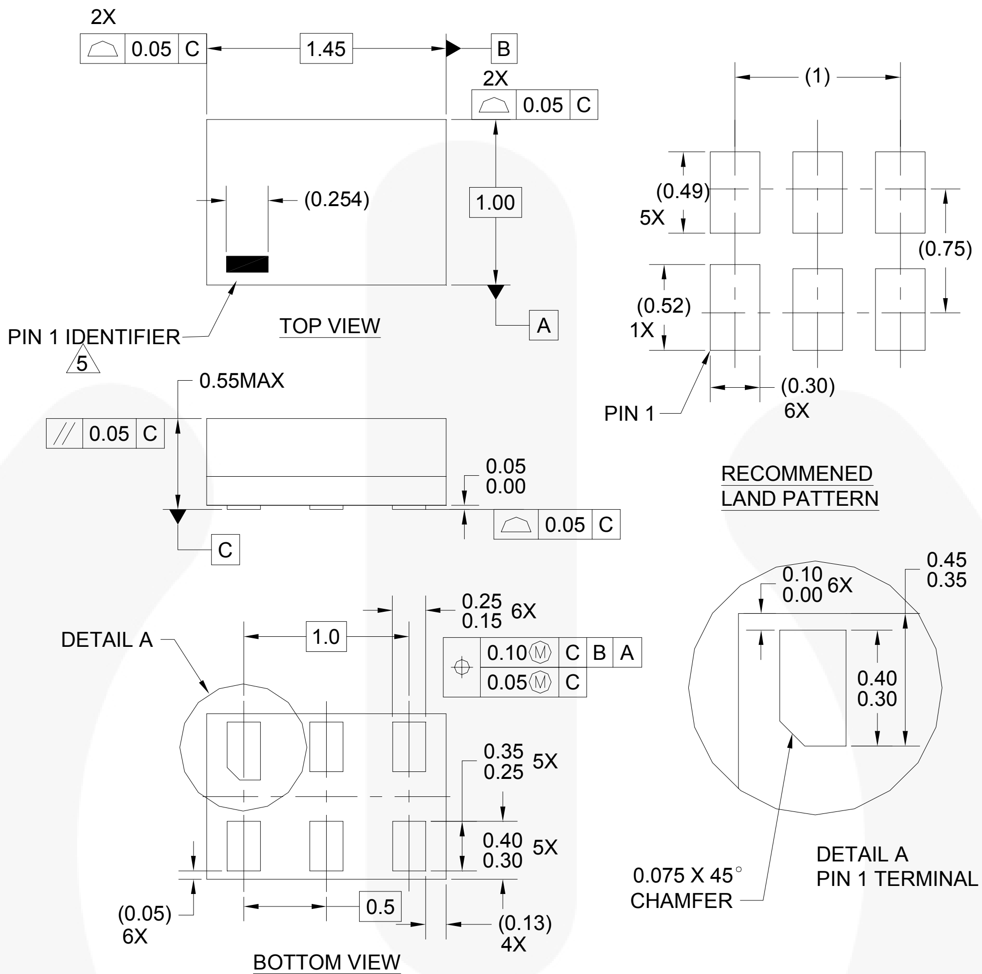
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/analog/pdf/sc70-6_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 18. 6-Lead, MicroPak™, 1.0mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: *http://www.fairchildsemi.com/packaging/.*

Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: *http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.*

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

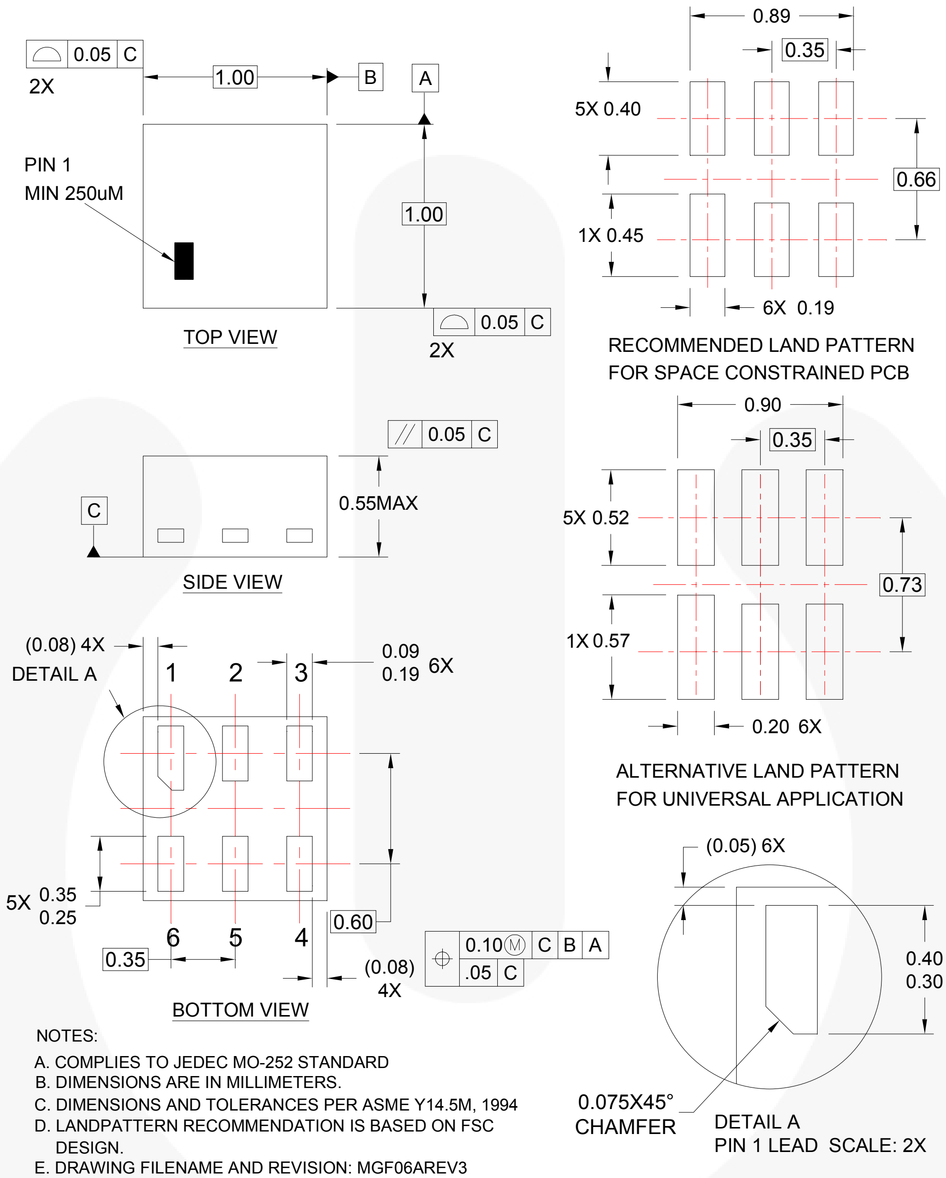


Figure 19. 6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch

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.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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