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## NC7SZ10 TinyLogic® UHS 3-Input NAND Gate

### General Description

The NC7SZ10 is a single 3-Input NAND Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad  $V_{CC}$  operating range. The device is specified to operate over the 1.65V to 5.5V  $V_{CC}$  operating range. The inputs and output are high impedance when  $V_{CC}$  is 0V. Inputs tolerate voltages up to 7V independent of  $V_{CC}$  operating voltage.

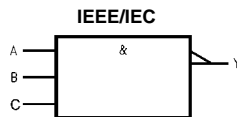
### Features

- Space saving SC70 6-lead package
- Ultra small MicroPak™ leadless package
- Ultra High Speed;  $t_{PD}$  2.4 ns typ into 50 pF at 5V  $V_{CC}$
- High Output Drive;  $\pm 24$  mA at 3V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range; 1.65V–5.5V
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

### Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ10P6X	MAA06A	Z10	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ10L6X	MAC06A	E6	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

### Logic Symbol



### Pin Descriptions

Pin Names	Description
A, B, C	Inputs
Y	Output

### Function Table

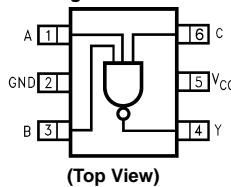
$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

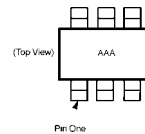
H = HIGH Logic Level  
L = LOW Logic Level  
X = Either LOW or HIGH Logic Level

### Connection Diagrams

#### Pin Assignments for SC70

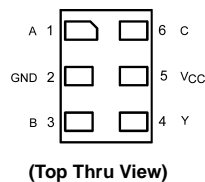


#### Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code  
**Note:** Orientation of Top Mark determines Pin One location. Read the Top Product Code Mark left to right, Pin One is the lower left pin (see diagram).

#### Pad Assignments for MicroPak



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**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
@ $V_{IN} < -0.5V$	-50 mA
@ $V_{IN} > 6V$	+20 mA
DC Output Diode Current ( $I_{OK}$ )	
@ $V_{OUT} < -0.5V$	-50 mA
@ $V_{OUT} > 6V, V_{CC} = GND$	+20 mA
DC Output Current ( $I_{OUT}$ )	$\pm 50$ mA
DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature under Bias ( $T_J$ )	150°C
Junction Lead Temperature ( $T_L$ ); (Soldering, 10 seconds)	260°C
Power Dissipation ( $P_D$ ) @ +85°C SC70-5	150 mW

**Recommended Operating Conditions** (Note 2)

Supply Voltage Operating ( $V_{CC}$ )	1.65V to 5.5V
Supply Voltage Data Retention ( $V_{CC}$ )	1.5V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC}$ @ 1.8V, 2.5V $\pm 0.2V$	0 ns/V to 20 ns/V
$V_{CC}$ @ 3.3V $\pm 0.3V$	0 ns/V to 10 ns/V
$V_{CC}$ @ 5.0V $\pm 0.5V$	0 ns/V to 5 ns/V
Thermal Resistance ( $\theta_{JA}$ ) SC70-5	425°C/W

**Note 1:** Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

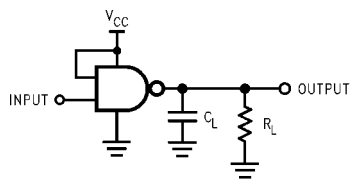
Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 $V_{CC}$ 0.70 $V_{CC}$			0.75 $V_{CC}$ 0.70 $V_{CC}$		V	
$V_{IL}$	LOW Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.25 $V_{CC}$ 0.30 $V_{CC}$			0.25 $V_{CC}$ 0.30 $V_{CC}$		V	
$V_{OH}$	HIGH Level Output Voltage	1.65 2.3 3.0 4.5	1.55 2.2 2.9 4.4	1.65 2.3 3.0 4.5	1.55 2.2 2.9 4.4		V	$V_{IN} = V_{IL}$ $I_{OH} = -100 \mu A$	
		1.65 2.3 3.0 4.5	1.29 1.9 2.4 3.8	1.52 2.15 2.80 4.20	1.29 1.9 2.4 3.8				
$V_{OL}$	LOW Level Output Voltage	1.65 2.3 3.0 4.5	0.0 0.0 0.0 0.1			0.1 0.1 0.1 0.1		V	$V_{IN} = V_{IH}$ $I_{OL} = 100 \mu A$
		1.65 2.3 3.0 4.5	0.08 0.10 0.15 0.22	0.24 0.3 0.4 0.55	0.24 0.3 0.4 0.55				
$I_{IN}$	Input Leakage Current	0 to 5.5	$\pm 1$			$\pm 10$		$\mu A$	$V_{IN} = 5.5V, GND$
$I_{OFF}$	Power Off Leakage Current	0.0	1			10		$\mu A$	$V_{IN}$ or $V_{OUT} = 5.5V$
$I_{CC}$	Quiescent Supply Current	1.65 to 5.5	2.0			20		$\mu A$	$V_{IN} = 5.5V, GND$

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	1.8 ± 0.15	2.0	7.0	17.5	2.0	18.0	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 MΩ	Figures 1, 3
		2.5 ± 0.2	0.8	3.0	10.5	0.8	11.0			
		3.3 ± 0.3	0.5	2.4	7.5	0.5	8.0			
		5.0 ± 0.5	0.5	2.0	5.5	0.5	6.0			
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	3.3 ± 0.3	1.5	2.9	8.5	1.5	9.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω	Figures 1, 3
		5.0 ± 0.5	0.8	2.4	7.5	0.8	8.0			
C <sub>IN</sub>	Input Capacitance	0	4					pF		
C <sub>PD</sub>	Power Dissipation Capacitance	3.3	24					pF	(Note 3)	Figure 2
		5.0	30							

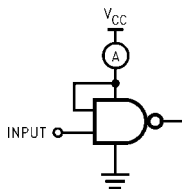
**Note 3:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2.) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:  
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$ .

## AC Loading and Waveforms



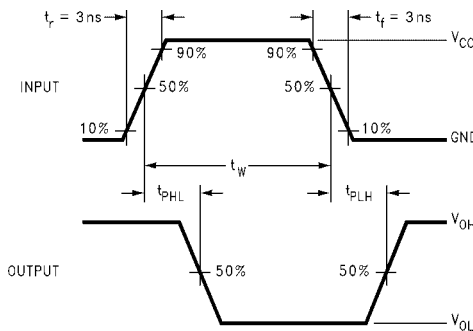
C<sub>L</sub> includes load and stray capacitance  
 Input PRR = 1.0 MHz; t<sub>w</sub> = 500 ns

**FIGURE 1. AC Test Circuit**



Input = AC Waveform; t<sub>r</sub> = t<sub>f</sub> = 1.8 ns;  
 PRR = 10 MHz; Duty Cycle = 50%

**FIGURE 2. I<sub>CCD</sub> Test Circuit**



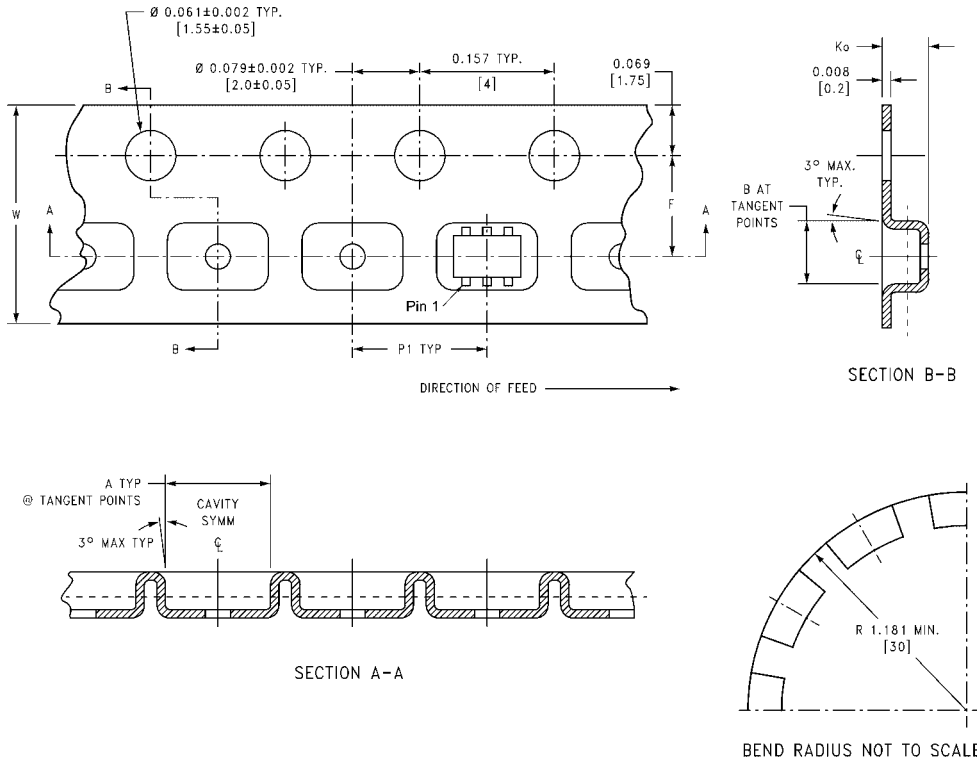
**FIGURE 3. AC Waveforms**

## Tape and Reel Specification

### Tape Format for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### TAPE DIMENSIONS inches (millimeters)

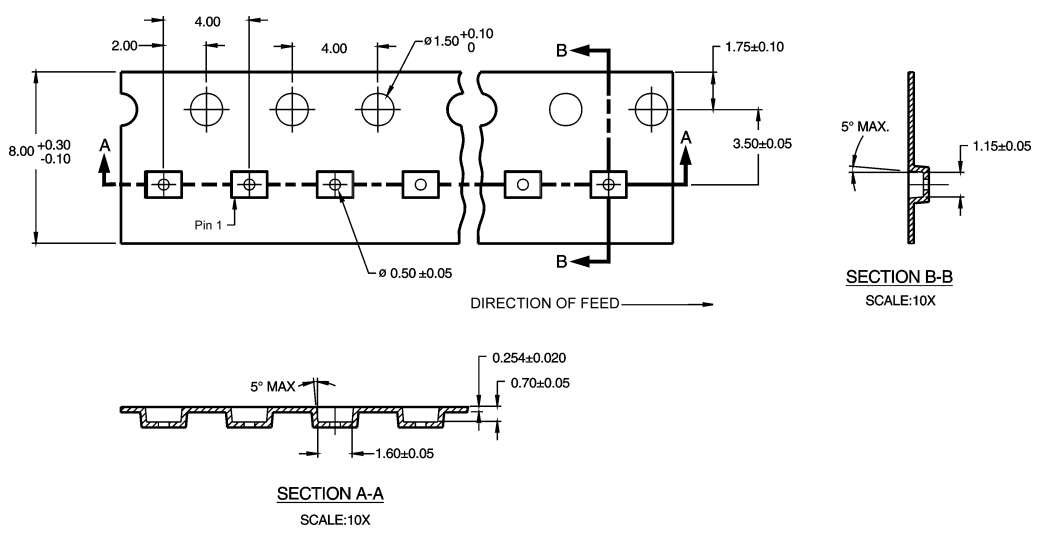


Package	Tape Size	DIM A	DIM B	DIM F	DIM $K_o$	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	$0.138 \pm 0.004$ (3.5 ± 0.10)	$0.053 \pm 0.004$ (1.35 ± 0.10)	0.157 (4)	$0.315 \pm 0.004$ (8 ± 0.1)

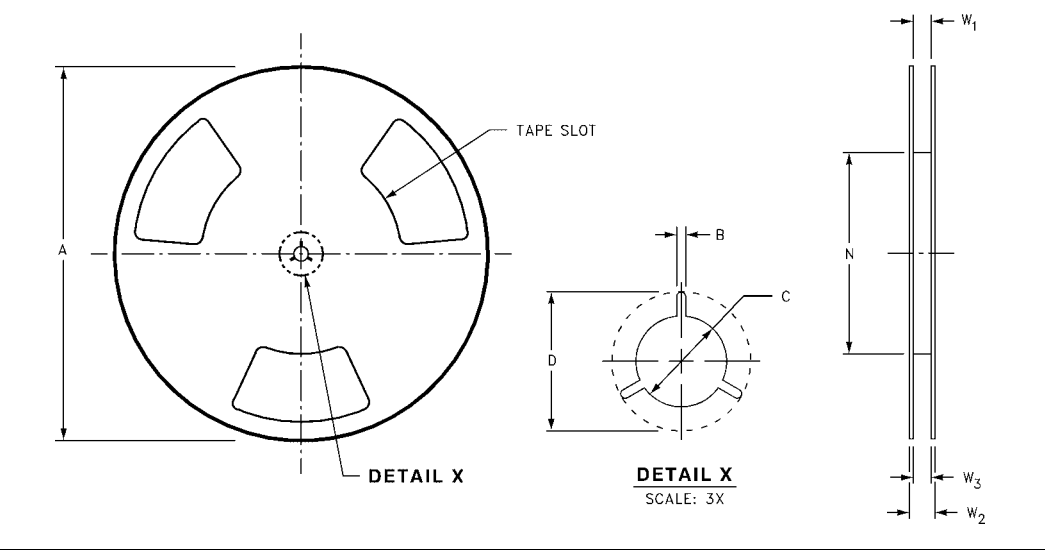
**Tape and Reel Specification** (Continued)

**Tape Format for MicroPak**

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed



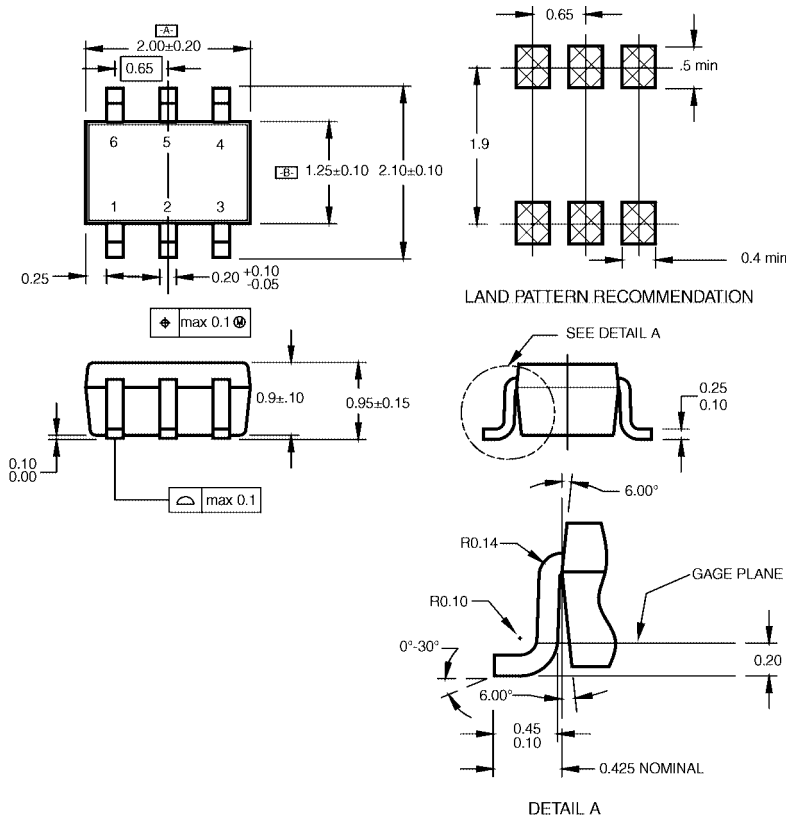
**REEL DIMENSIONS** inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

NC7SZ10

**Physical Dimensions** inches (millimeters) unless otherwise noted

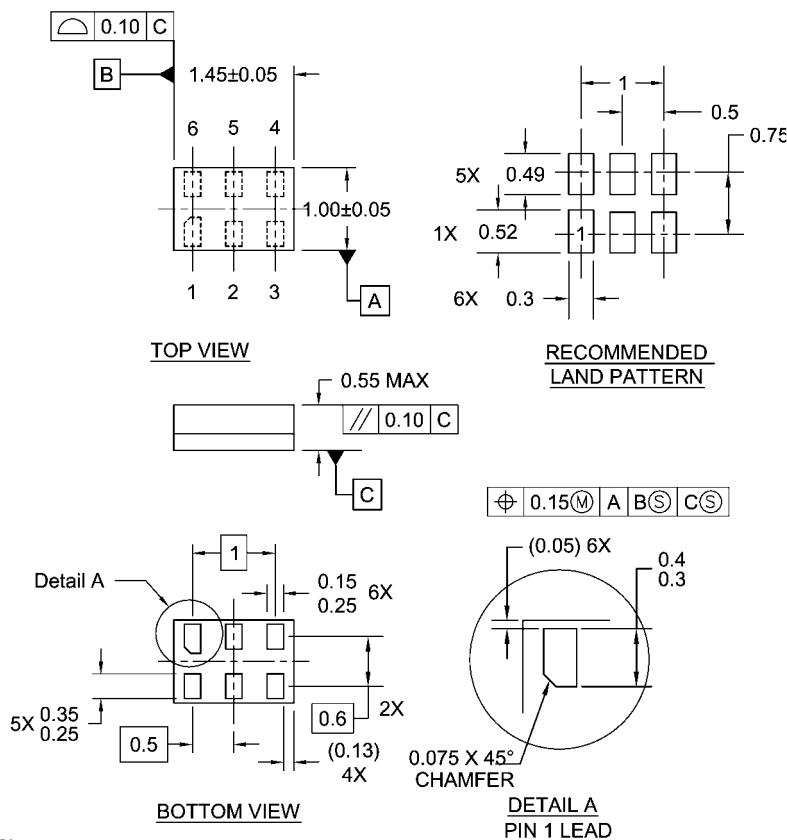


NOTES:  
 A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.  
 B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.  
 C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

**6-Lead SC70, EIAJ SC88, 1.25mm Wide  
 Package Number MAA06A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**Notes:**

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide  
Package Number MAC06A**

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