PCA9511A

Hot Swappable I²C-Bus and SMBus Bus Buffer

The PCA9511A is a hot swappable I²C−bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9511A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PCA9511A rise time accelerator circuitry allows the use of weaker DC pull−up currents while still meeting rise time requirements. The PCA9511A incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open−drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

During insertion, the PCA9511A SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

Features

- Bidirectional Buffer for SDA and SCL Lines Increases Fan−Out and Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Multipoint Backplane Systems
- ΔV/Δt Rise Time Accelerators on all SDA and SCL lines
- Active HIGH ENABLE Input
- Active HIGH READY Open−Drain Output
- High−Impedance SDA and SCL for V_{CC} = 0 V
- 1 V precharge on all SDA and SCL Lines
- Supports Clock Stretching and Multiple Master arbitration/Synchronization
- V_{CC} Operating Range: 2.7 V to 5.5 V
- I²C and SMBus SCL Clock Frequency up to 1 MHz
- Alternate Features for PCA9510A/PCA9512A/PCA9513A/PCA9514A
- Available in: Micro8, SOIC−8
- ESD Performance: 8000 V HBM, 600 V MM, 2000V CDM
- These are Pb−Free Devices

Applications

- cPCI, VME, AdvancedTCA cards and other multipoint backplane cards that are required to be inserted or removed from an operating system

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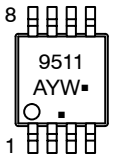
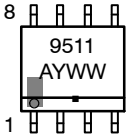
MARKING DIAGRAMS

Micro8™
DM SUFFIX
CASE 846A



SOIC−8
CASE 751



A = Assembly Location
L = Wafer Lot
M = Date Code
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

FEATURE SELECTION

FEATURE SELECTION CHART

Feature	PCA9510A	PCA9511A	PCA9512A	PCA9513A	PCA9514A
idle detect	Yes	Yes	Yes	Yes	Yes
high−impedance SDA, SCL pins for V_{CC} = 0 V	Yes	Yes	Yes	Yes	Yes
rise time accelerator circuitry on SDAn and SCLn lines		Yes	Yes	Yes	Yes
rise time accelerator circuitry hardware disable pin for lightly loaded systems			Yes		
rise time accelerator threshold 0.8 V versus 0.6 V improves noise margin				Yes	Yes
ready open−drain output	Yes	Yes		Yes	Yes
two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins			Yes		
1 V precharge on all SDA and SCL lines	In only	Yes	Yes		
92 μA current source on SCLIN and SDAIN for PICMG applications				Yes	

BLOCK DIAGRAM

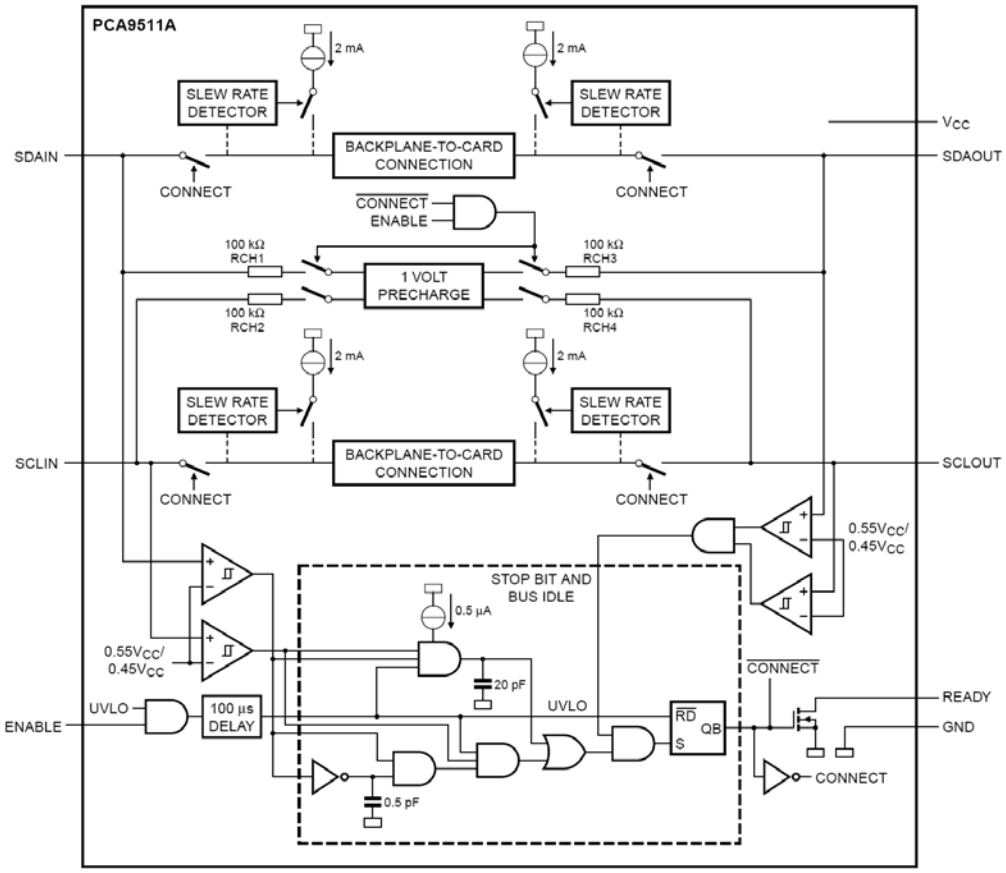


Figure 1. Block Diagram of PCA9511A

PIN ASSIGNMENT

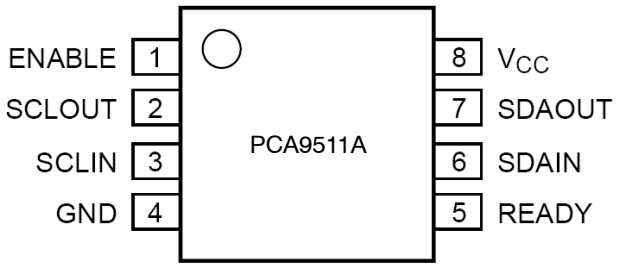


Figure 2. SOIC8 / Micro−8

PIN DESCRIPTIONS

Symbol	Pin	Description
ENABLE	1	Chip enable. Grounding this input puts the part in a low current (< 1 μA) mode. It also disables the rise time accelerators, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
SCLOUT	2	Serial Clock Output to and from the SCL bus on the card
SCLIN	3	Serial Clock Input to and from the SCL bus on the backplane
GND	4	Ground. Connect this pin to a ground plane for best results.
READY	5	Open−drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and goes HIGH when the two sides are connected Port.
SDAIN	6	Serial Data Input to and from the SDA bus on the backplane
SDAOUT	7	Serial Data Output to and from the SDA bus on the card
V_{CC}	8	Supply Voltage

FUNCTIONAL DESCRIPTION

Please refer to Figure 1 “Block Diagram of PCA9511A”.

Start−up

An undervoltage / initialization circuit holds the parts in a disconnected state which presents high−impedance to all SDA and SCL pins during power−up. A LOW on the ENABLE pin also forces the parts into the low current disconnected state when the I_{CC} is essentially zero. As the power supply is brought up and the ENABLE is HIGH or the part is powered and the ENABLE is taken from LOW to HIGH, it enters an initialization state where the internal references are stabilized and the precharge circuit is enabled. At the end of the initialization state, the ‘Stop Bit And Bus Idle’ detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state (t_{en}) and remaining HIGH when all the SDA and SCL pins have been HIGH for the bus idle time or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. The 1 V precharge circuitry is activated during the initialization and is deactivated when the connection is made. The precharge circuitry pulls up the SDA and SCL pins to 1 V through individual 100 kΩ nominal resistors. This precharges the pins to 1 V to minimize the worst case disturbances that result from inserting a card into the backplane where the backplane and the card are at opposite logic levels.

Connect Circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT, as well as SCLIN and SCLOUT, become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between $0.7V_{CC}$ and V_{CC} is generally ignored because a falling edge is only recognized when it falls below $0.7\ V_{CC}$ with a slew rate of at least 1.25 V/μs. When a falling edge is seen on one pin, the other pin in the pair turns on a pull−down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below $0.7\ V_{CC}$. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate, then the initial pull−down rate will continue. If the first falling pin has a slow slew rate, then the second pin will be pulled down

at its initial slew rate only until it is just above the first pin voltage, then they will both continue down at the slew rate of the first.

Once both sides are LOW, they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value, for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise until the internal driver pulls it down to the offset voltage. When the last external driver stops driving a LOW, that pin will rise up and settle out just above the other pin, as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/μs, when the pin voltage exceeds 0.6 V for the PCA9511A, the rise time accelerator's circuits are turned on and the pull−down driver is turned off.

Maximum Number of Devices in Series

Each buffer adds about 0.1 V dynamic level offset at 25°C with the offset larger at higher temperatures. Maximum offset (V_{offset}) is 0.150 V with a 10 kΩ pull−up resistor. The LOW level at the signal origination end (master) is dependent upon the load, and the only specification point is that the I^2C−bus specification of 3 mA will produce V_{OL} < 0.4 V, although if lightly loaded, the V_{OL} may be ~0.1 V. Assuming V_{OL} = 0.1 V and V_{offset} = 0.1 V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care, a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator, thus introducing false clock edges. Generally, it is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

The PCA9510A (rise time accelerator is permanently disabled) and the PCA9512A (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns on the accelerator turns the pull−down off. If the V_{IL} is above ~0.6 V and a rising edge is detected, the pull−down will turn off and will not turn back on until a falling edge is detected.

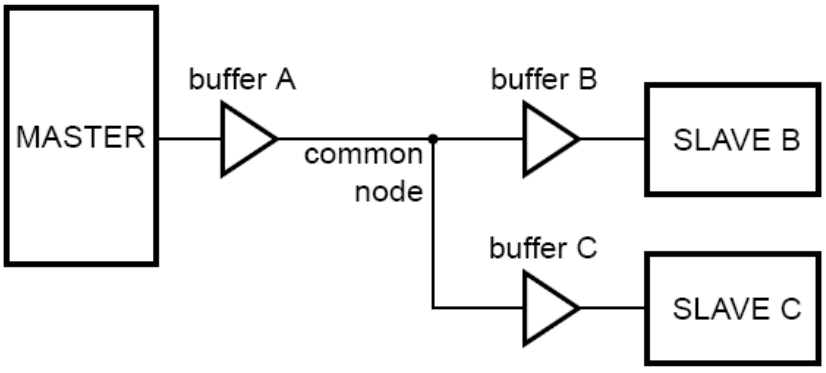


Figure 3. System with 3 Buffers Connected to Common Node

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 3. Consider if the V_{OL} at the input of buffer A is 0.3 V and the V_{OL} of Slave B (when acknowledging) is 0.4 V, with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change, you would observe V_{IL} at the input of buffer A of 0.3 V and its output, the common node, is ~0.4 V. The output of buffer B and buffer C would be ~0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is ~0.5 V. When the Master pull−down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before buffer B's output turns on, if the pull−up is strong, the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V, the accelerators on both buffer A and buffer C will fire contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while, the rising edge accelerators will turn off and the common node will return to ~0.5 V because the buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6 V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

Propagation Delays

The delay for a rising edge is determined by the combined pull−up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull−up currents are the same, any difference in rise time is directly proportional to the difference in

capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below 0.7 V_{CC}, and the output turn on has a non−zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up, it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn−on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature, V_{CC} and process, as well as the load current and the load capacitance.

Rise Time Accelerators

During positive bus transitions, a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PCA9511A is exceeded. The rising edge rate should be at least 1.25 V/μs to guarantee turn on of the accelerators. The built−in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines require the bus pull−up voltage and supply voltage (V_{CC}) to be the same.

READY Digital Output

This pin provides a digital flag which is LOW when either ENABLE is LOW, or the start−up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is HIGH and start−up is complete. The pin is driven by an open−drain pull−down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 kΩ to V_{CC} to provide the pull−up.

ENABLE Low Current Disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise time accelerators, drives READY LOW, disables the bus precharge circuitry, and puts the part in a low current state. When the pin voltage is driven all the way to V_{CC}, the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

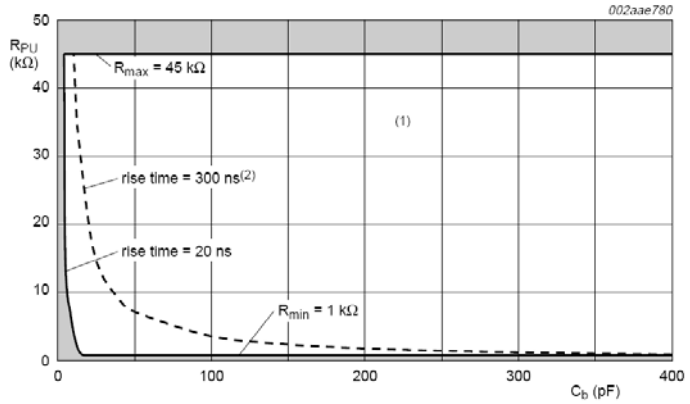
Resistor Pull−Up Value Selection

The system pull−up resistors must be strong enough to provide a positive slew rate of 1.25 V/μs on the SDA and SCL pins, in order to activate the boost pull−up currents during rising edges. Choose maximum resistor value using the formula given below:

$$R_{PU} \leq 800 \times 10^3 \left(\frac{V_{CC(min)} - 0.6}{C} \right)$$

where R_{PU} is the pull−up resistor value in Ω, $V_{CC(min)}$ is the minimum V_{CC} voltage in volts, and C is the equivalent bus capacitance in picofarads (pF).

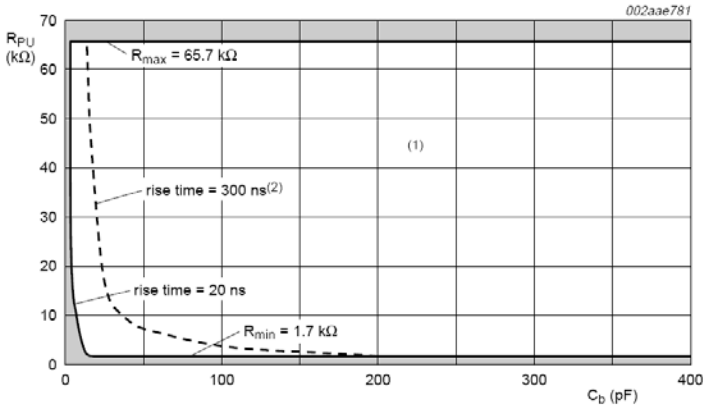
In addition, regardless of the bus capacitance, always choose $R_{PU} \leq 65.7$ kΩ for $V_{CC} = 5.5$ V maximum, $R_{PU} \leq 45$ kΩ for $V_{CC} = 3.6$ V maximum. The start−up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull−up values are needed to overcome the precharge voltage. See the curves in Figures 4 and 5 for guidance in resistor pull−up selection.



(1) Unshaded area indicates recommended pull-up, for rise time < 300 ns, with PCA9511A.
(2) Rise time without PCA9511A.

(1) Unshaded area indicates recommended pull−up, for rise time < 300 ns, with PCA9511A.
(2) Rise time without PCA9511A.

Figure 4. Bus Requirements for 3.3 V Systems



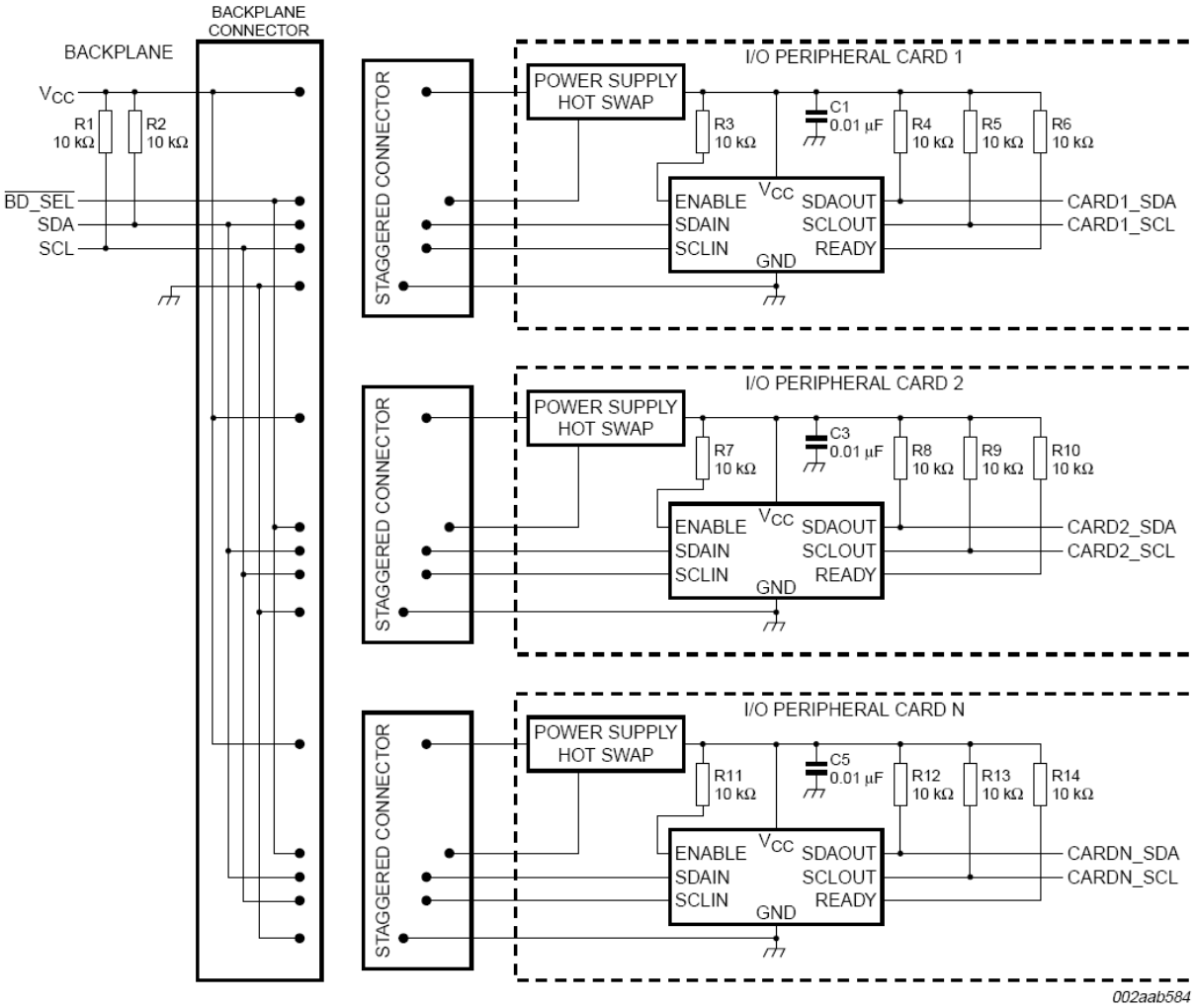
(1) Unshaded area indicates recommended pull-up, for rise time < 300 ns, with PCA9511A.
(2) Rise time without PCA9511A.

(1) Unshaded area indicates recommended pull−up, for rise time < 300 ns, with PCA9511A.
(2) Rise time without PCA9511A.

Figure 5. Bus Requirements for 5 V Systems

Hot Swapping and Capacitance Buffering Application

Figures 6 through 9 illustrate the usage of the PCA9511A in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9511A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.



Remark: The PCA9511A can be used in any combination depending on the number of rise time accelerators that are needed by the system. Normally only one PCA9511A would be required per bus.

Figure 6. Hot Swapping multiple I/O Cards into a Backplane using the PCA9511A in a cPCI, VME and AdvancedTCA System

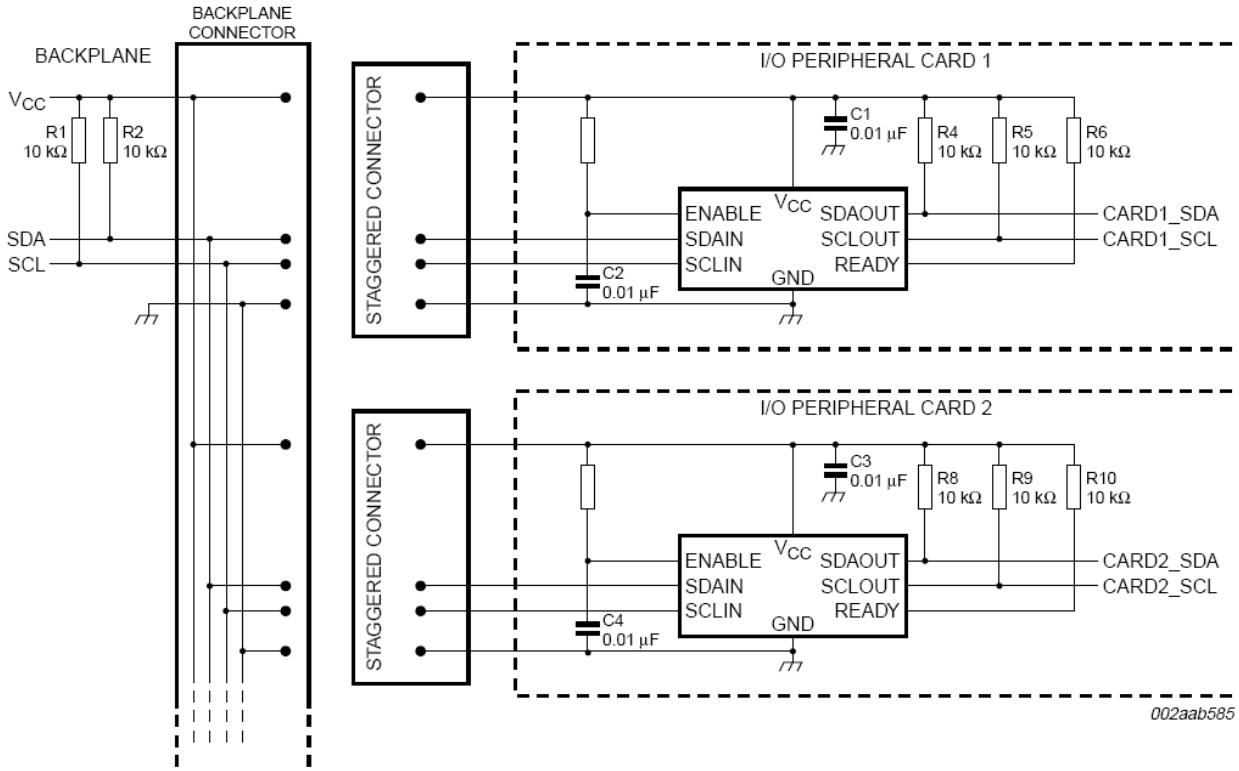


Figure 7. Hot Swapping Multiple I/O Cards into a Backplane Using the PCA9511A in a PCI System

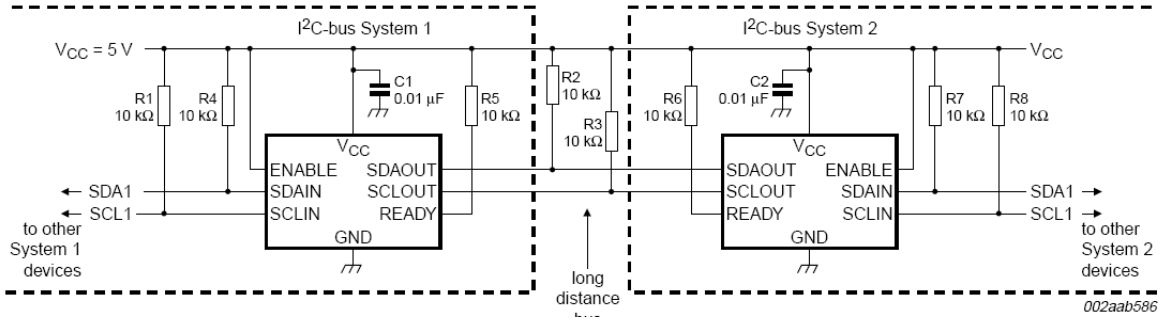
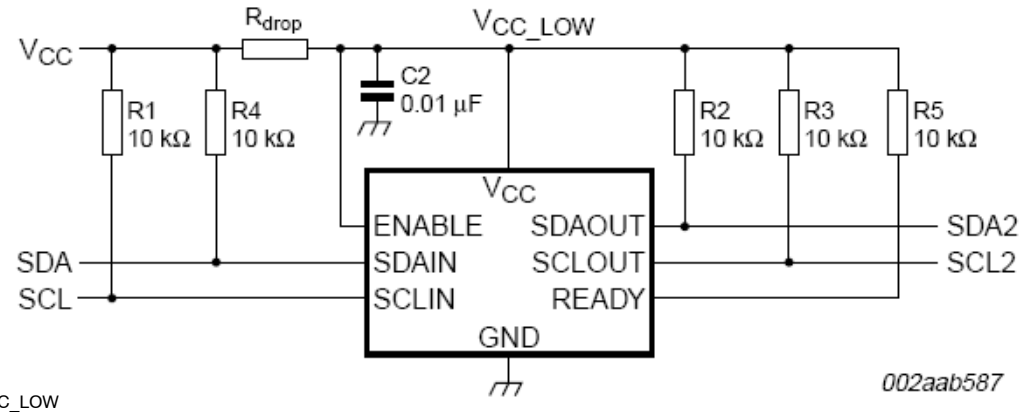


Figure 8. Repeater / Bus Extender Application using the PCA9511A



$V_{CC} > V_{CC\_LOW}$
R_{drop} is the line loss of VCC in the backplane.

Figure 9. System with Disparate V_{CC} Voltages

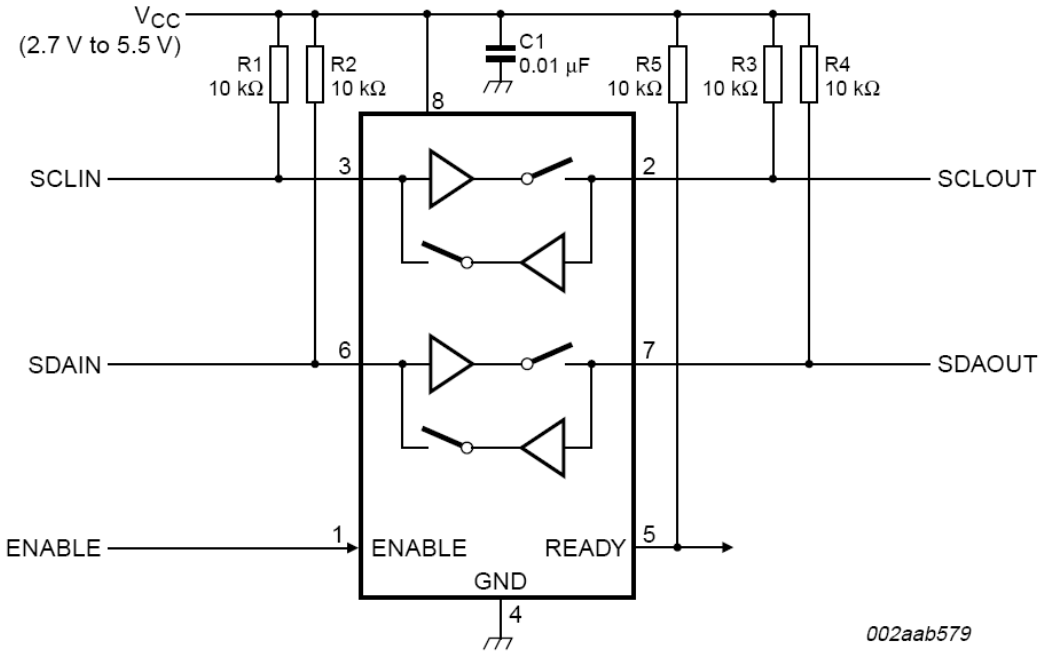


Figure 10. Typical Application

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		−0.5 to +7.0	V
V_n	Input / Output Voltage SDAIN, SCLIN, SDAOUT, SCLOUT, READY, ENABLE		−0.5 to +7.0	V
I_I	Input Current		±20	mA
I_O	Output Current		±50	mA
I_{CC}	DC Supply Current		±100	mA
I_{GND}	DC Ground Current		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
θ_{JA}	Thermal Resistance	SOIC8 (Note 1) Micro8	146 205	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC8 Micro8	856 609	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Mode (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 8000 > 600 > 2000	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22−A114−A.
3. Tested to EIA / JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	2.7	5.5	V
V_n	Input / Output Voltage	0	5.5	V
T_A	Operating Free−Air Temperature	−40	+85	°C

CHARACTERISTICS V_{CC} = 2.7 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_A = −40°C to +85°C			Unit
			Min	Typ	Max	
SUPPLIES						
I_{CC} (Note 6)	Supply Current	V_{CC} = 5.5 V; V_{SDAIN} = V_{SCLIN} = 0 V		3.5	6	mA
$I_{CC(sd)}$	Shutdown Mode Supply Current	V_{ENABLE} = 0 V; All other pins at V_{CC} or GND		0.1		μA
START−UP CIRCUITRY						
V_{pch} (Note 6)	Precharge Voltage	SDA, SCL Floating	0.8	1.1	1.2	V
$V_{IH(ENABLE)}$	High−Level Input Voltage		0.7 x V_{CC}			V
$V_{IL(ENABLE)}$	Low−Level Input Voltage				0.3 x V_{CC}	V
$I_{I(ENABLE)}$	Input Current on pin ENABLE	V_{ENABLE} = 0 V to V_{CC}		±0.1	±1	μA
t_{en} (Note 7)	Enable Time			110		μs
$t_{idle(READY)}$ (Note 6)	Bus Idle Time to READY Active		50	105	200	μs
$t_{dis(EN−RDY)}$	Disable Time (ENABLE to READY)			30		ns
$t_{stp(READY)}$ (Note 8)	SDAIN to READY delay after STOP			1.2		μs
t_{READY} (Note 8)	SCLOUT/SDAOUT to READY delay			0.8		μs
$I_{LZ(READY)}$	Off−State Leakage Current on pin READY	V_{ENABLE} = V_{CC}		±0.3		μA
$C_{I(ENABLE)}$ (Note 9)	Input Capacitance on pin ENABLE	V_I = V_{CC} or GND		1.9	4	pF
$C_{O(READY)}$ (Note 9)	Input Capacitance on pin ENABLE	V_I = V_{CC} or GND		2.5	4	pF
$V_{OL(READY)}$ (Note 6)	Low−Level Output Voltage on pin READY	V_{ENABLE} = V_{CC}; I_{pu} = 3 mA			0.4	V
RISE TIME ACCELERATORS						
$I_{trt(pu)}$ (Notes 10, 11)	Transient Boosted Pull−up Current	Positive transition on SDA, SCL; V_{CC} = 2.7 V; Slew rate = 1.25 V/μs	1	2		mA
INPUT−OUTPUT CONNECTION						
V_{offset} (Notes 6, 12, 13)	Offset Voltage	10 kΩ to V_{CC} on SDA, SCL; V_{CC} = 3.3 V	0	110	175	mV
t_{PLH}	Low to High Propagation Delay	SCL to SCL and SDA to SDA; 10 kΩ to V_{CC}; C_L = 100 pF each side		0		ns
t_{PHL}	High to Low Propagation Delay	SCL to SCL and SDA to SDA; 10 kΩ to V_{CC}; C_L = 100 pF each side		70		ns
I_{LI}	Input Leakage Current	SDAn, SCLn pins; V_{CC} = 5.5 V			±1	μA
$C_{I(SCL/SDA)}$ (Note 9)	SCL and SDA Input Capacitance			5	7	pF
V_{OL} (Note 6)	Low−Level Output Voltage	V_I = 0 V; SDAn, SCLn pins; I_{sink} = 3 mA, V_{CC} = 2.7 V			0.4	V

6. This specification applies over the full operating temperature range.
7. The enable time can slow considerably for some parts when temperature is < −20°C.
8. Delays that can occur after ENABLE and/or idle times have passed.
9. Guaranteed by design, not production tested.
10. $I_{trt(pu)}$ varies with temperature and V_{CC} voltage, as shown in the "Typical performance characteristics" section.
11. Input pull−up voltage should not exceed power supply voltage in operating mode because the rise time accelerator will clamp the voltage to the positive supply rail.
12. The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull−up resistor and V_{CC} voltage is shown in the "Typical performance characteristics" section.
13. Force V_{SDAIN} = V_{SCLIN} = 0.1 V, tie SDAOUT and SCLOUT through 10 kΩ resistor to V_{CC} and measure the SDAOUT and SCLOUT output.

SYSTEM CHARACTERISTICS V_{CC} = 2.7 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_A = −40°C to +85°C				Unit
			Min	Max	Min	Max	
f_{SCL} (Note 14)	SCL Clock Frequency		0	400	0	1000	kHz
t_{BUF} (Note 14)	Bus Free Time Between a STOP and START Condition		1.3		0.5		μs
$t_{HD;STA}$ (Note 14)	Hold Time (Repeated) START Condition		0.6		0.26		μs
$t_{SU;STA}$ (Note 14)	Setup Time for a Repeated START Condition		0.6		0.26		μs
$t_{SU;STO}$ (Note 14)	Setup Time for STOP Condition		0.6		0.26		μs
$t_{HD;DAT}$ (Note 14)	Data Hold Time		300		120		ns
$t_{SU;DAT}$ (Note 14)	Data Setup Time		100		50		ns
t_{LOW} (Note 14)	LOW Period of SCL		1.3		0.5		μs
t_{HIGH} (Note 14)	HIGH Period of SCL		0.6		0.26		μs
t_f (Note 14)	Fall Time of SDA and SCL		20 + 0.1 x C_b (Note 15)	300	–	120	ns
t_r (Note 14)	Rise Time of SDA and SCL		20 + 0.1 x C_b (Note 15)	300	–	120	ns

14. Guaranteed by design, not production tested.
15. C_b = total capacitance of one bus line in pF.

TYPICAL PERFORMANCE CHARACTERISTICS

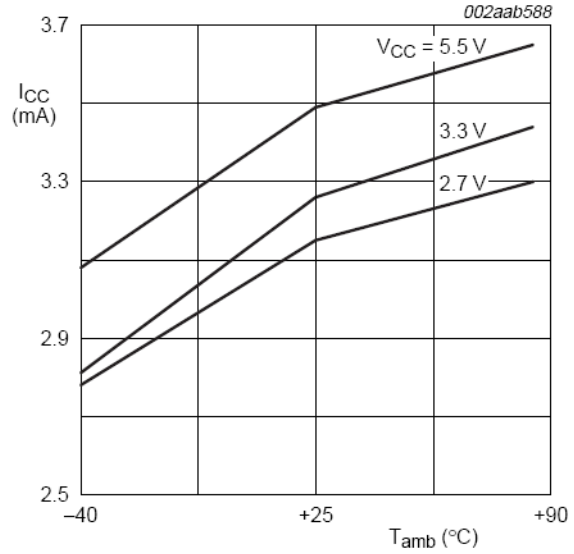


Figure 11. I_{CC} vs. Temperature

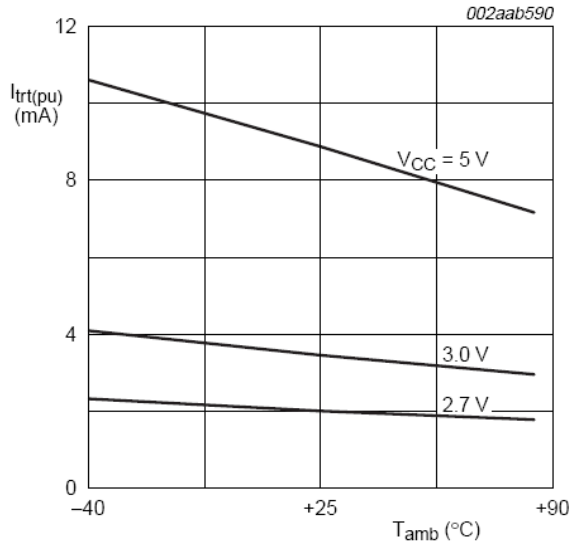
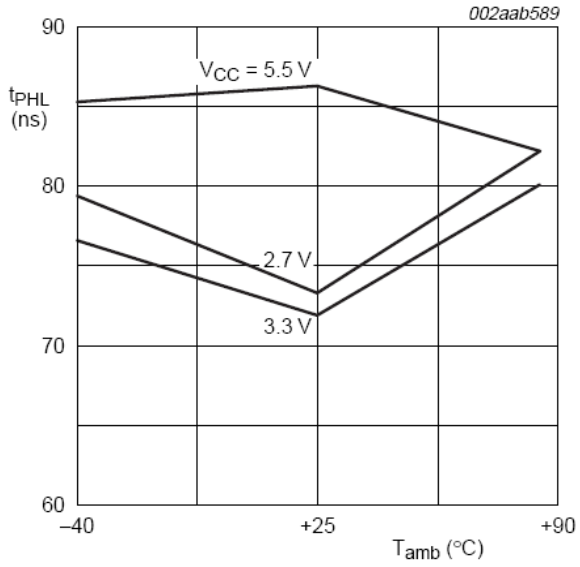


Figure 12. $I_{trt(pu)}$ vs. Temperature



$C_i = C_o > 100$ pF; $R_{PU(in)} = R_{PU(out)} = 10$ kΩ

Figure 13. Input/Out t_{PHL} vs. Temperature

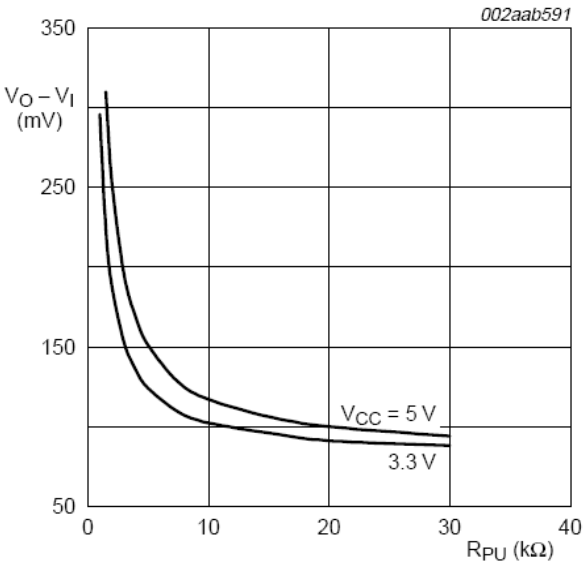


Figure 14. Connection Circuitry $V_O - V_I$

TIMING DIAGRAMS

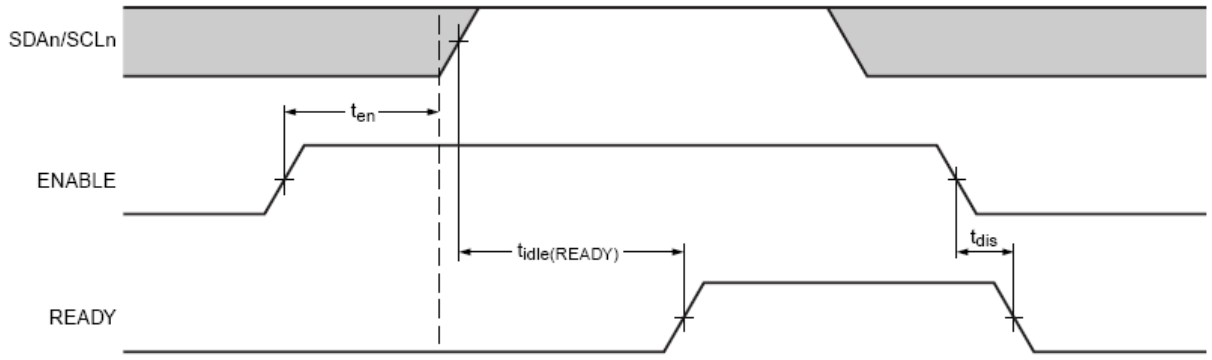
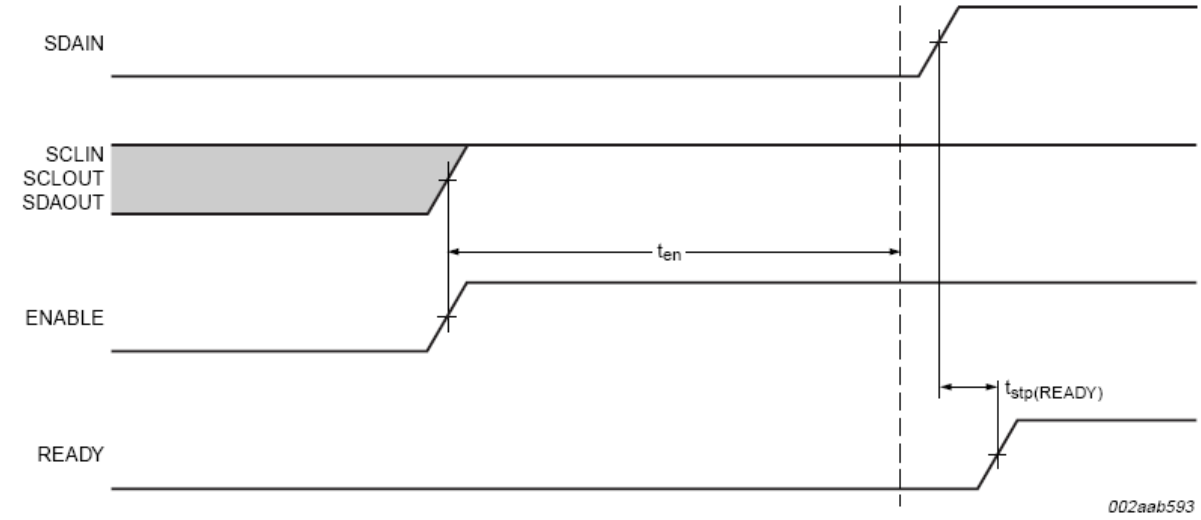
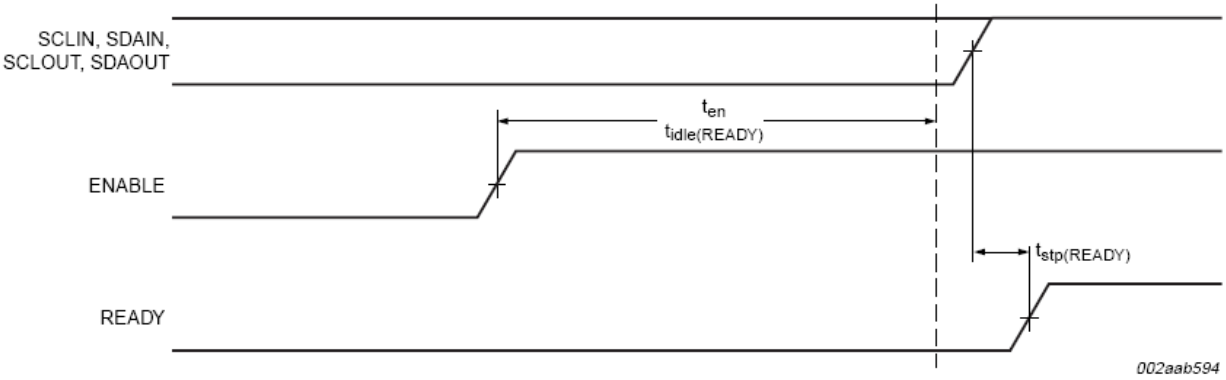


Figure 15. Timing for t_{en}, $t_{idle(READY)}$ and t_{dis}



$t_{stp(READY)}$ is only applicable after the t_{en} delay.

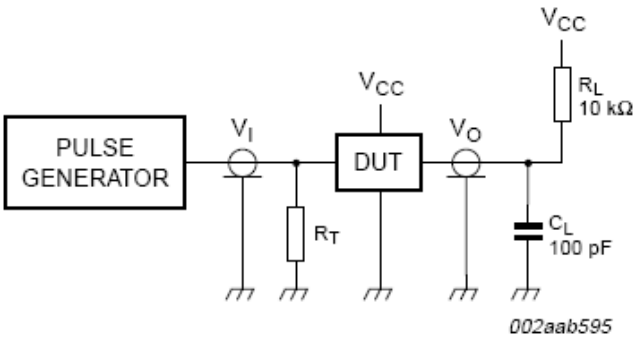
Figure 16. $t_{stp(READY)}$ That Can Occur After t_{en}



$t_{stp(READY)}$ is only applicable after the t_{en} delay.

Figure 17. $t_{stp(READY)}$ Delay that Can Occur After t_{en} and $t_{idle(READY)}$

TEST SETUP



R_L = load resistor

C_L = load capacitance includes jig and probe capacitance

R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generators.

Figure 18. Test Circuitry for Switching Times

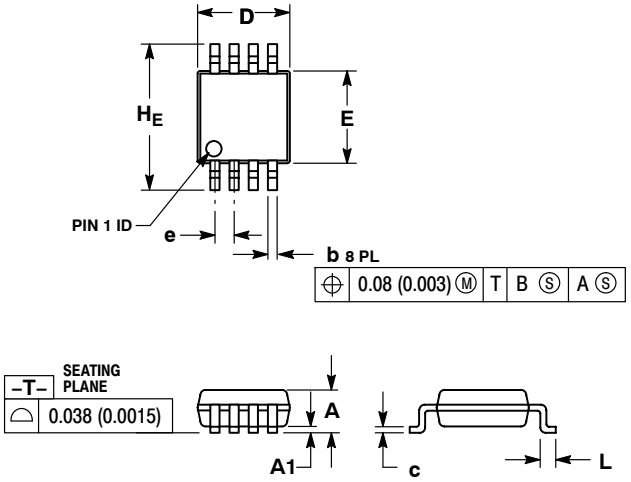
ORDERING INFORMATION

Device	Package	Shipping
PCA9511ADR2G In Development	SOIC8 (Pb−Free)	3000 / Tape & Reel
PCA9511ADMR2G	Micro−8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

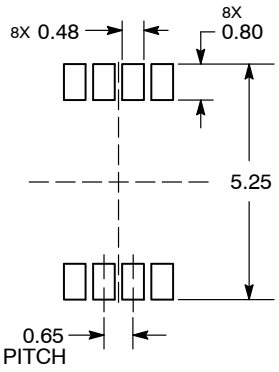
Micro8™
CASE 846A–02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A–01 OBSOLETE, NEW STANDARD 846A–02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	––	––	1.10	––	––	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65 BSC			0.026 BSC	
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

RECOMMENDED SOLDERING FOOTPRINT*

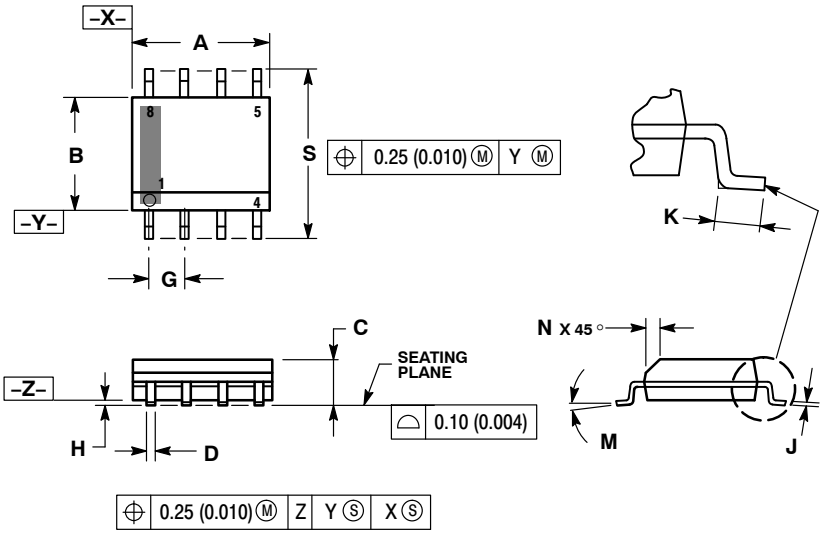


DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

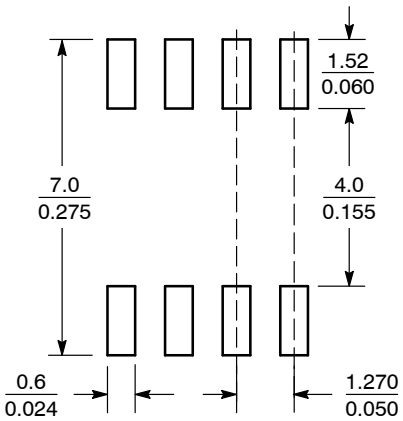
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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