100-Tap Digital Potentiometer (DP) with Buffered Wiper

Description

The DP7111 is a single digital potentiometer (DP) designed as an electronic replacement for mechanical potentiometers. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The DP7111 contains a 100−tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_{WB}. The DP7111 wiper is buffered by an op amp that operates rail to rail. The wiper setting, stored in non−volatile memory, is not lost when the device is powered down and is automatically recalled when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper−control of the DP7111 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digital potentiometer can be used as a buffered voltage divider. For applications where the potentiometer is used as a 2−terminal variable resistor, please refer to the DP7113. The buffered wiper of the DP7111 is not compatible with that application.

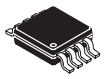
Features

- 100−position Linear Taper Potentiometer
- Non−volatile EEPROM Wiper Storage; Buffered Wiper
- Low Power CMOS Technology
- Single Supply Operation: 2.5 V – 6.0 V
- Increment Up/Down Serial Interface
- Resistance Values: 10 kΩ, 50 kΩ and 100 kΩ
- Available in SOIC, TSSOP and MSOP Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

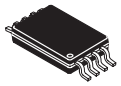
Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Tamper−proof Calibrations
- Contrast, Brightness and Volume Controls
- Motor Controls and Feedback Systems
- Programmable Analog Functions

SOIC−8

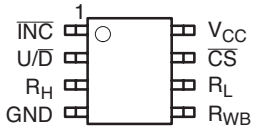


MSOP−8



TSSOP−8

PIN CONFIGURATIONS



SOIC (V),
MSOP (Z)

TSSOP (Y)
(Top Views)

PIN FUNCTION

Pin Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_{WB}	Buffered Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

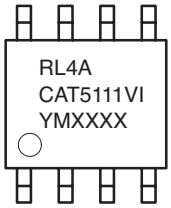
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

~~August, 2010 − Rev. 18~~ Jun, 2017 Rev. 19
Publication Order Number:
DP7111/~~D~~

DEVICE MARKING INFORMATION

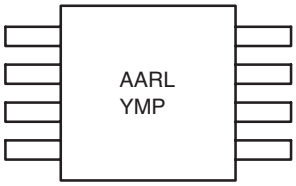
SOIC



R = Resistance:
- 2 = 10 kΩ
- 4 = 50 kΩ
- 5 = 100 kΩ

L = Assembly Location
4 = Lead Finish – NiPdAu
A = Product Revision (Fixed as “A”)
CAT5111V = Device Code
I = Temperature Range (Industrial)
Y = Production Year (Last Digit)
M = Production Month
(1–9, A, B, C or O, N, D)
XXXX = Last Four Digits of Assembly Lot Number

MSOP



AARL = DP7111ZI–10–T3
AAPT = DP7111ZI–50–T3
AAPX = DP7111ZI–00–T3
Y = Production Year (Last Digit)
M = Production Month
(1–9, A, B, C or O, N, D)
P = Product Revision

TSSOP

A1 = Device Code
R = Resistance:
- 2 = 10 kΩ
- 4 = 50 kΩ
- 5 = 100 kΩ

L = Assembly Location
4 = Lead Finish – NiPdAu
Y = Production Year (Last Digit)
M = Production Month
(1–9, A, B, C or O, N, D)
XXX = Last Three Digits of
Assembly Lot Number

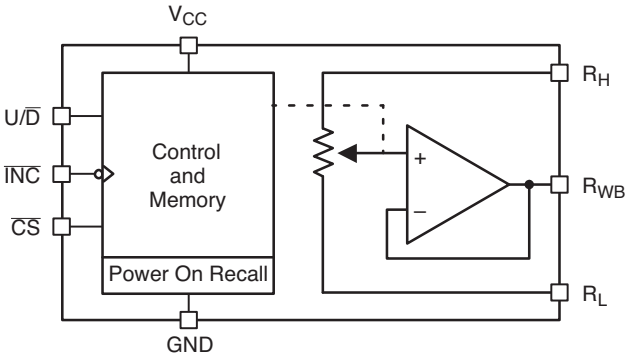


Figure 1. Functional Diagram

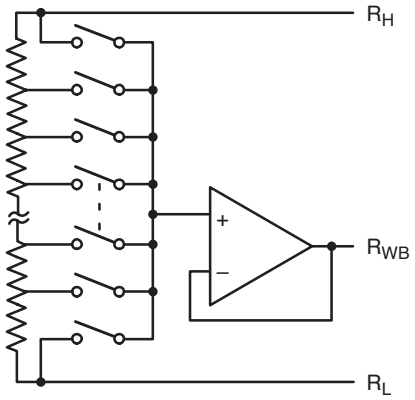


Figure 2. Electronic Potentiometer Implementation

Pin Description

$\overline{\text{INC}}$: Increment Control Input

The $\overline{\text{INC}}$ input (on the falling edge) moves the wiper in the up or down direction determined by the condition of the U/$\overline{\text{D}}$ input.

U/$\overline{\text{D}}$: Up/Down Control Input

The U/$\overline{\text{D}}$ input controls the direction of the wiper movement. When in a high state and $\overline{\text{CS}}$ is low, any high−to−low transition on $\overline{\text{INC}}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{\text{CS}}$ is low, any high−to−low transition on $\overline{\text{INC}}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_{WB}: Wiper Potentiometer Terminal (Buffered)

R_{WB} is the buffered wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, $\overline{\text{INC}}$, U/$\overline{\text{D}}$ and $\overline{\text{CS}}$.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{\text{CS}}$: Chip Select

The chip select input is used to activate the control input of the DP7111 and is active low. When in a high state, activity on the $\overline{\text{INC}}$ and U/$\overline{\text{D}}$ inputs will not affect or change the position of the wiper.

Device Operation

The DP7111 operates like a digital potentiometer with R_H and R_L equivalent to the high and low terminals and R_{WB} equivalent to the mechanical potentiometer's wiper. There are 100 available tap positions including the resistor end points, R_H and R_L. There are 99 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs, $\overline{\text{INC}}$, U/$\overline{\text{D}}$ and $\overline{\text{CS}}$. These inputs control a seven−bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{\text{INC}}$ and $\overline{\text{CS}}$ inputs.

With $\overline{\text{CS}}$ set LOW the DP7111 is selected and will respond to the U/$\overline{\text{D}}$ and $\overline{\text{INC}}$ inputs. HIGH to LOW transitions on $\overline{\text{INC}}$ will increment or decrement the wiper (depending on the state of the U/$\overline{\text{D}}$ input and seven−bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{\text{CS}}$ transitions HIGH while the $\overline{\text{INC}}$ input is also HIGH. When the DP7111 is powered−down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{\text{INC}}$ set low, the DP7111 may be de−selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

Table 1. OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward R_H
High to Low	Low	Low	Wiper toward R_L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby

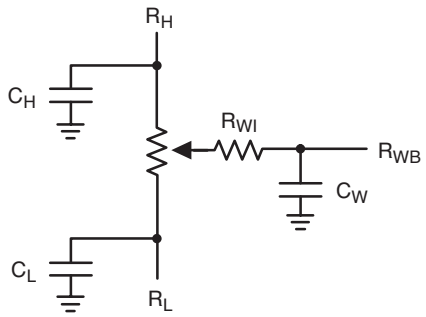


Figure 3. Potentiometer Equivalent Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage V_{CC} to GND	–0.5 to +7	V
Inputs $\overline{CS}$ to GND	–0.5 to V_{CC} +0.5	V
$\overline{INC}$ to GND	–0.5 to V_{CC} +0.5	V
U/$\overline{D}$ to GND	–0.5 to V_{CC} +0.5	V
R_H to GND	–0.5 to V_{CC} +0.5	V
R_L to GND	–0.5 to V_{CC} +0.5	V
R_{WB} to GND	–0.5 to V_{CC} +0.5	V
Operating Ambient Temperature Industrial ('I' suffix)	–40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	–65 to 150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP} (Note 1)	ESD Susceptibility	MIL–STD–883, Test Method 3015	2000			V
I_{LTH} (Notes 1, 2)	Latch–Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL–STD–883, Test Method 1008	100			Years
N_{END}	Endurance	MIL–STD–883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch–up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} + 1 V

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V to +6 V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.5	–	6	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6 V, f = 1 MHz, I_W = 0	–	–	200	μA
		V_{CC} = 6 V, f = 250 kHz, I_W = 0	–	–	100	μA
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 6 V	–	–	1000	μA
		V_{CC} = 3 V	–	–	500	μA
I_{SB1} (Note 4)	Supply Current (Standby)	$\overline{CS}$ = V_{CC} – 0.3 V U/$\overline{D}$, $\overline{INC}$ = V_{CC} – 0.3 V or GND	–	75	150	μA
LOGIC INPUTS						
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	–	–	10	μA
I_{IL}	Input Leakage Current	V_{IN} = 0 V	–	–	–10	μA
V_{IH1}	TTL High Level Input Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V	2	–	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	–	0.8	V
V_{IH2}	CMOS High Level Input Voltage	2.5 V ≤ V_{CC} ≤ 6 V	V_{CC} x 0.7	–	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		–0.3	–	V_{CC} x 0.2	V
POTENTIOMETER CHARACTERISTICS						
R_{POT}	Potentiometer Resistance	–10 Device		10		kΩ
		–50 Device		50		
		–00 Device		100		
	Pot. Resistance Tolerance				±20	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			1		%
INL	Integral Linearity Error	I_W ≤ 2 μA		0.5	1	LSB
DNL	Differential Linearity Error	I_W ≤ 2 μA		0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance	0.05 V_{CC} ≤ V_{WB} ≤ 0.95 V_{CC}, V_{CC} = 5 V			1	Ω
I_{OUT}	Buffer Output Current	0.05 V_{CC} ≤ V_{WB} ≤ 0.95 V_{CC}, V_{CC} = 5 V			3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC				20	ppm/°C
$C_{RH}/C_{RL}/C_{RW}$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10 kΩ		1.7		MHz
$V_{WB(SWING)}$	Output Voltage Range	I_{OUT} ≤ 100 μA, V_{CC} = 5 V	0.01 V_{CC}		0.99 V_{CC}	

3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Latch–up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} + 1 V
5. I_W = source or sink
6. These parameters are periodically sampled and are not 100% tested.

Table 5. AC TEST CONDITIONS

V_{CC} Range	2.5 V ≤ V_{CC} ≤ 6 V
Input Pulse Levels	0.2 V_{CC} to 0.7 V_{CC}
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V_{CC}

Table 6. AC OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +6.0 V, V_H = V_{CC}, V_L = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100	–	–	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	–	–	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	–	–	ns
t_{IL}	$\overline{INC}$ LOW Period	250	–	–	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	–	–	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	–	–	μs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	–	–	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	–	–	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	–	1	5	μs
t_{CYC}	$\overline{INC}$ Cycle Time	1	–	–	μs
t_R, t_F (Note 8)	$\overline{INC}$ Input Rise and Fall Time	–	–	500	μs
t_{PU} (Note 8)	Power−up to Wiper Stable	–	–	1	ms
t_{WR}	Store Cycle	–	5	10	ms

7. Typical values are for T_A = 25°C and nominal supply voltage.
8. This parameter is periodically sampled and not 100% tested.

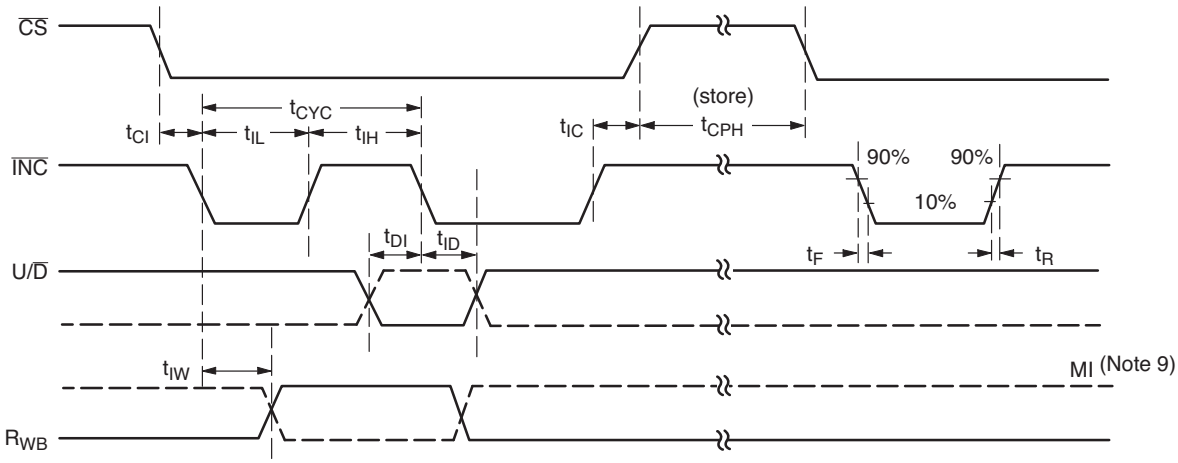
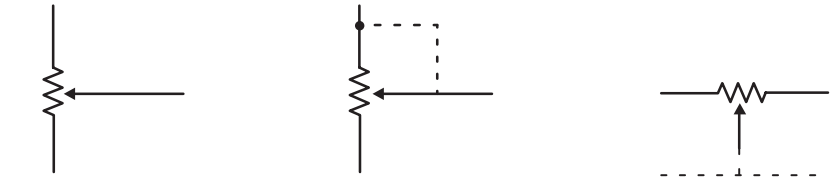


Figure 4. A.C. Timing

9. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

Applications Information



(a) resistive divider (b) variable resistance (c) two–port

Figure 5. Potentiometer Configuration

Applications

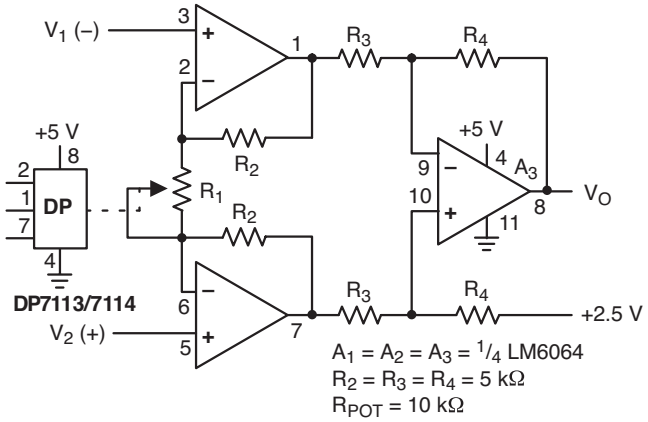


Figure 6. Programmable Instrumentation Amplifier

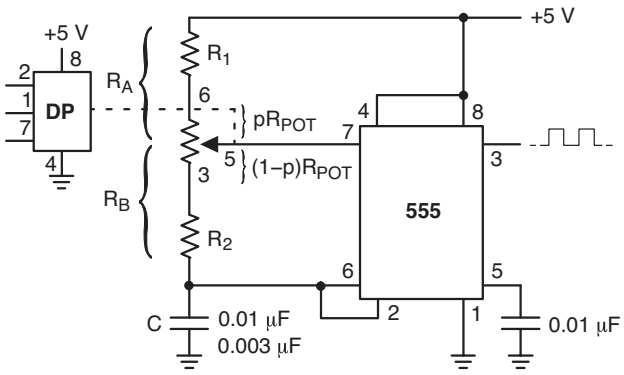


Figure 7. Programmable Sq. Wave Oscillator (555)

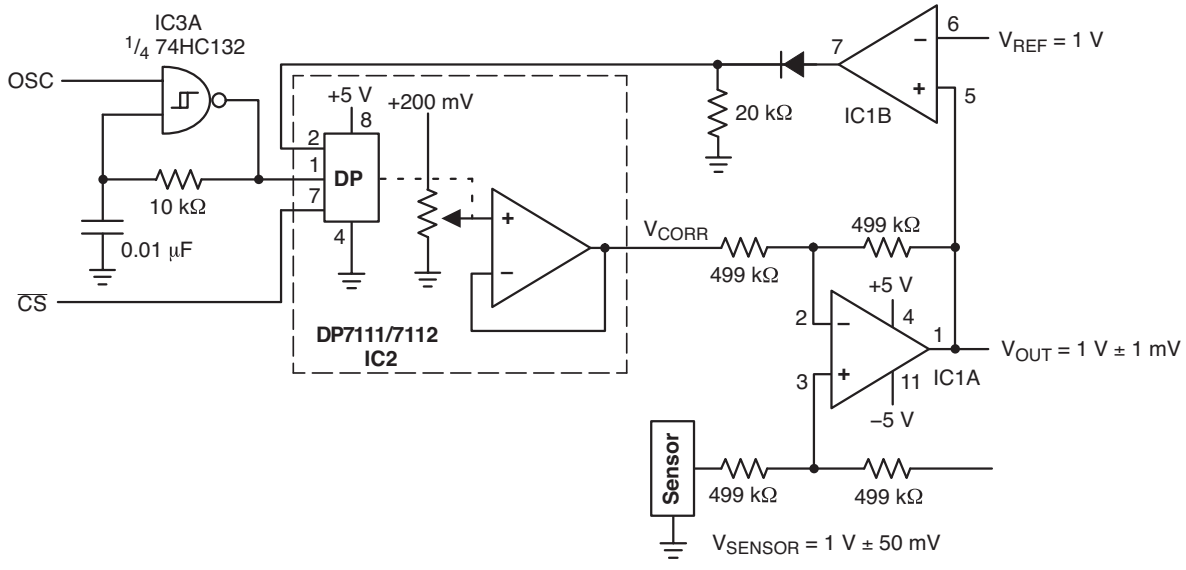


Figure 8. Sensor Auto Referencing Circuit

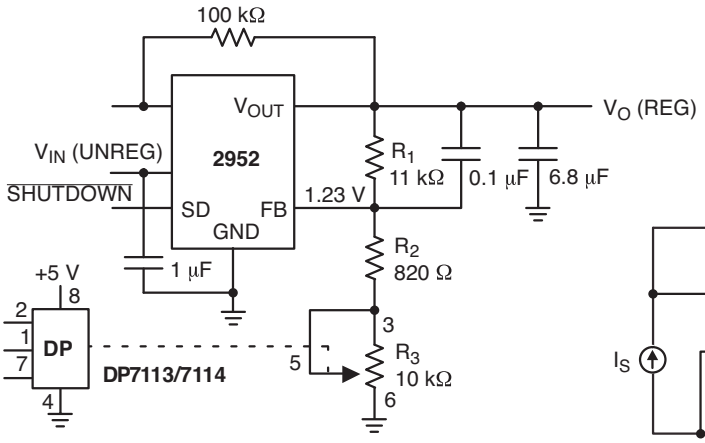


Figure 9. Programmable Voltage Regulator

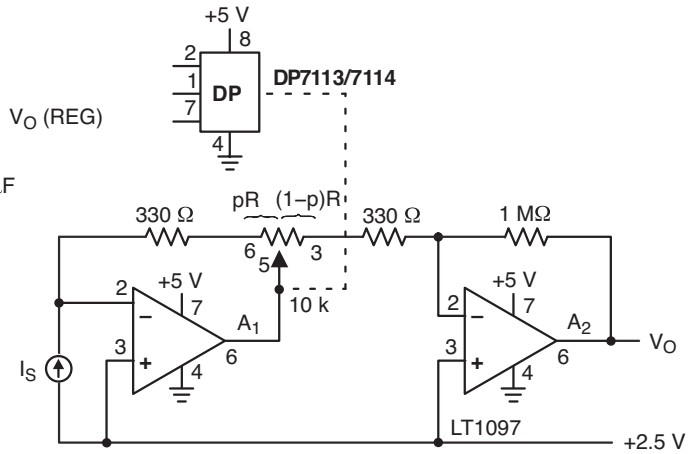


Figure 10. Programmable I to V Converter

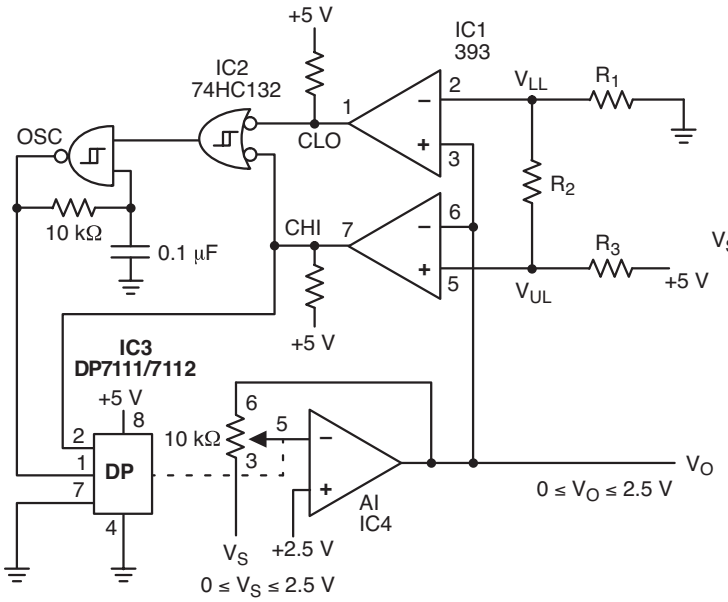


Figure 11. Automatic Gain Control

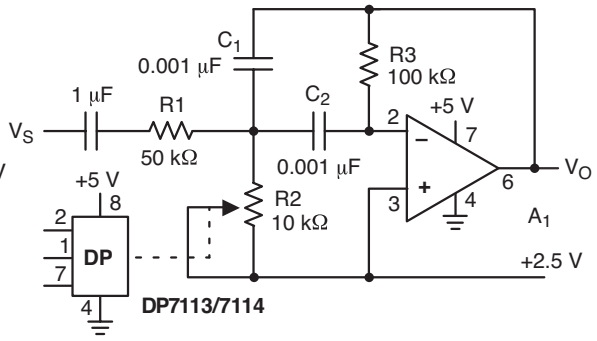


Figure 12. Programmable Bandpass Filter

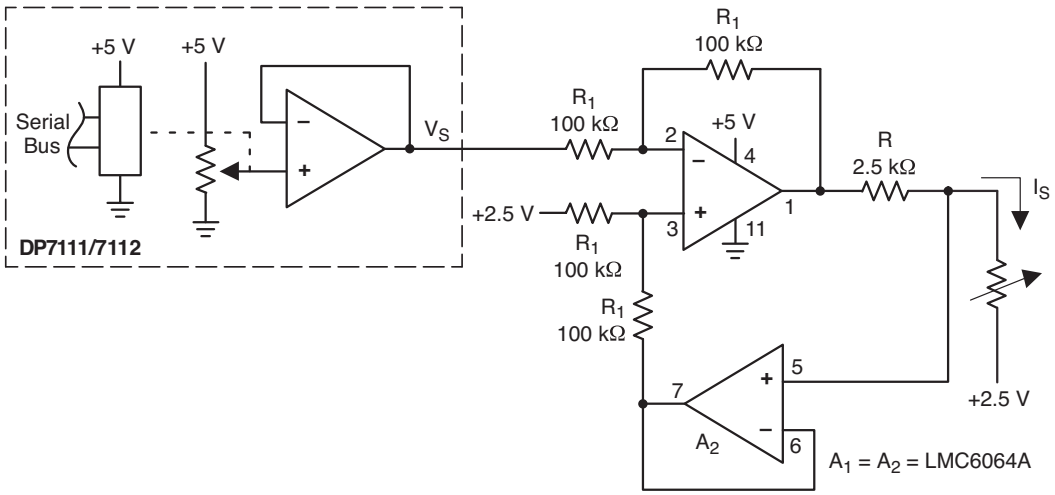
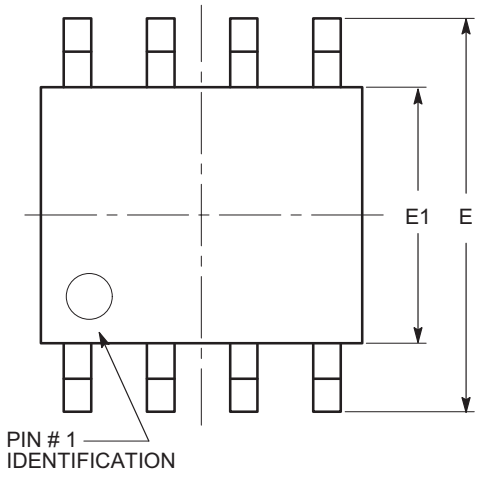


Figure 13. Programmable Current Source/Sink

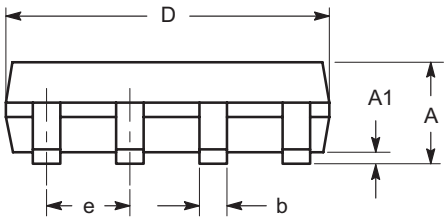
PACKAGE DIMENSIONS

SOIC 8, 150 mils

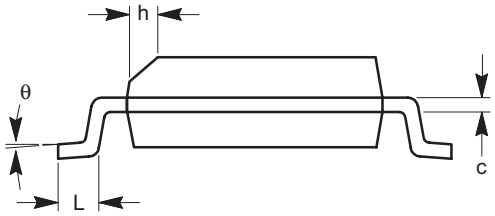


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



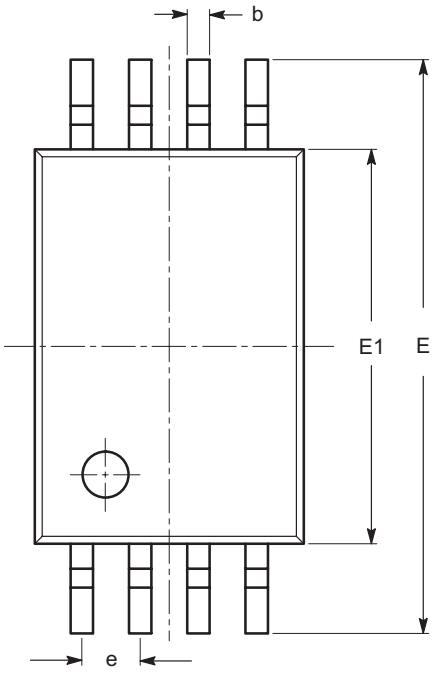
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

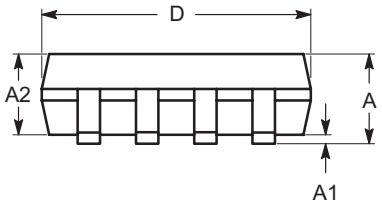
PACKAGE DIMENSIONS

TSSOP8, 4.4x3

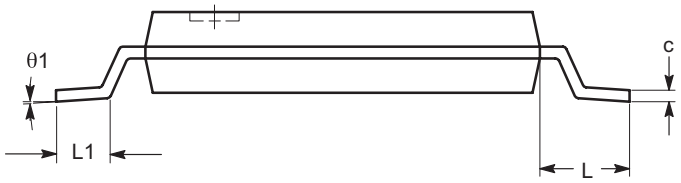


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW



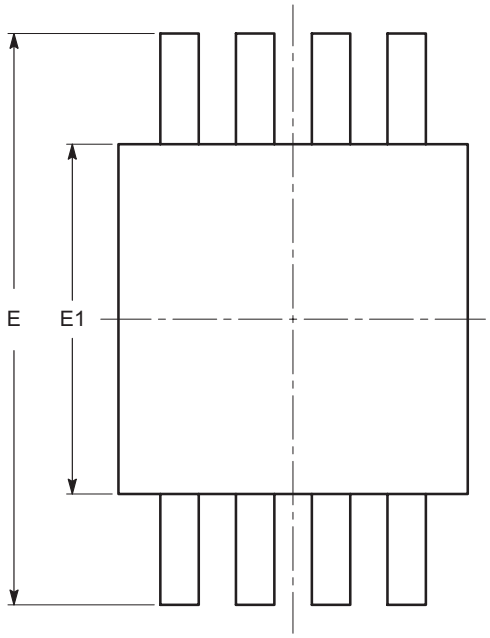
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

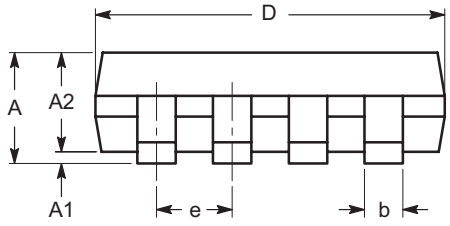
PACKAGE DIMENSIONS

MSOP 8, 3x3

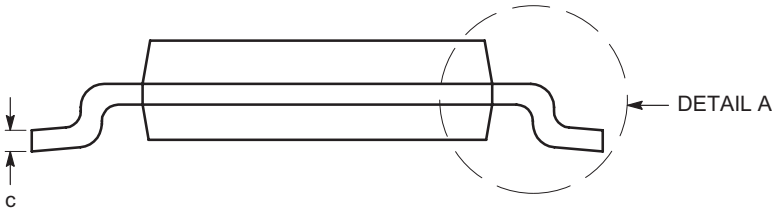


TOP VIEW

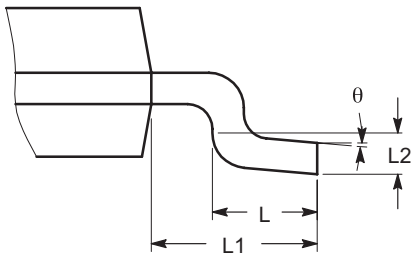
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°		6°



SIDE VIEW



END VIEW



DETAIL A

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

Example of Ordering Information (Note 12)

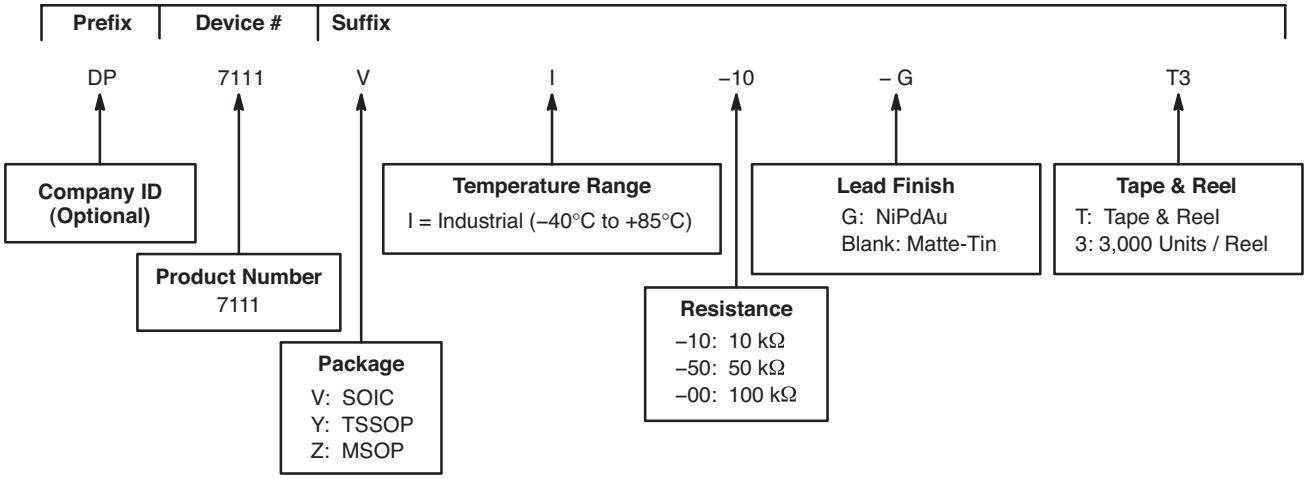


Table 7. ORDERING INFORMATION (Note 13)

Orderable Part Number	Resistance (kΩ)	Package–Pins	Lead Finish
DP7111VI–10–GT3	10	SOIC–8	NiPdAu
DP7111VI–50–GT3	50		
DP7111VI–00–GT3	100		
DP7111YI–10–GT3	10	TSSOP–8	NiPdAu
DP7111YI–50–GT3	50		
DP7111YI–00–GT3	100		
DP7111ZI–10–T3	10	MSOP–8	Matte-Tin
DP7111ZI–50–T3	50		
DP7111ZI–00–T3	100		

10. All packages are RoHS compliant.
11. Standard lead finish is NiPdAu, except MSOP package is Matte-Tin.
12. The device used in the above example is a DP7111VI–10–GT3 (SOIC, Industrial Temperature, 10 kΩ, NiPdAu, Tape & Reel, 3,000/Reel).
13. Contact factory for package availability.