NSi1050

Isolated CAN Transceiver

Datasheet (EN) 1.3

Product Overview

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050 device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps, and it can support at least 110 CAN nodes. The NSi1050 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000Vrms Insulation voltage
- Power supply voltage

  VDD1: 2.5V to 5.5V

  VDD2: 4.5V to 5.5V
- Bus fault protection of -40V to +40V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Date rate: up to 1Mbps
- High CMTI: 100kV/us
- Low loop delay: <200ns
- High system level EMC performance:

  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:

  SOW16

  DUB8

Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

Device Information

Part Number	*Package*	*Body Size*
NSI1050-DDBR	DUB8	9.30mm ×6.40mm
NSI1050-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

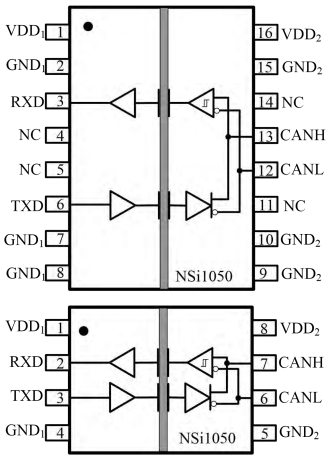

Figure 1. NSi1050 Block Diagram

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1.0 PIN CONFIGURATION AND FUNCTIONS

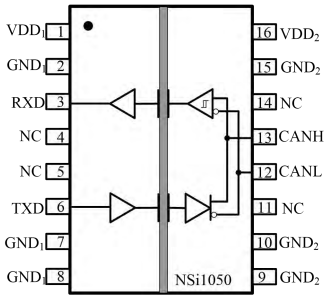


Figure 1.1 NSi1050-DSWR Package

Table1.1 NSi1050-DSWR Pin Configuration and Description

NSi1050-DSWR PIN NO.	SYMBOL	FUNCTION
1	VDD_1	Power Supply for Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	NC	No Connection
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Bus Side
10	GND_2	Ground 2, the ground reference for Isolator Bus Side
11	NC	No Connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No Connection
15	GND_2	Ground 2, the ground reference for Isolator Bus Side
16	VDD_2	Power supply for Bus Side

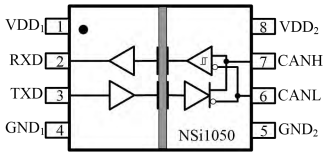


Figure 1.2 NSi1050-DDBR Package

Table1.2 NSi1050-DDBR Pin Configuration and Description

NSi1050-DDBR PIN NO.	SYMBOL	FUNCTION
1	VDD_1	Power Supply for Side 1
2	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
3	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD_2	Power supply for Bus Side

2.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD_1 ,VDD_2	-0.5		6.5	V	
Maximum Input Voltage	V_{TXD}	-0.4		VDD_1+0.4	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-40		+40	V	
Output current	Io	-15		15	mA	
Operating Temperature	Topr	-40		125	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3.0 RECOMMENDED OPERATING CONDITIONS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply voltage, controller side	V_{CC1}	2.5		5.5	V	
Supply voltage, bus side	V_{CC2}	4.5	5	5.5	V	
Voltage at bus pins (separately or common mode)	V_I or V_{IC}	-12		12	V	
High-level input voltage	V_{IH}	2		5.25	V	TXD
Low-level input voltage	V_{IL}	0		0.8	V	TXD
High-level output current	I_{OH}	-70			mA	Driver
		-4			mA	Receiver
Low-level output current	I_{OL}			70	mA	Driver
				4	mA	Receiver

Ambient Temperature	T_A	-40		125	℃	
Junction temperature	T_J	-40		150	℃	

4.0 THERMAL INFORMATION

Parameters	*Symbol*	*DUB8*	*SOW16*	*Unit*
Junction-to-ambient thermal resistance	θ_{JA}	73.3	76.0	℃/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	63.2	41	
Junction-to-board thermal resistance	θ_{JB}	43.0	47.7	

5.0 SPECIFICATIONS

5.1. ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage	VDD_1	2.5		5.5	V	
	VDD_2	4.5	5	5.5	V	
Logic side supply current	IDD_1		1.97	3.00	mA	VDD_1=3.3V, TXD=0
			0.97	1.50	mA	VDD_1=3.3V, TXD=VCC1
			2.02	3.00	mA	VDD_1=5V, TXD=0
			1.02	1.50	mA	VDD_1=5V, TXD=VCC1
Bus side supply current	IDD_2		46	70	mA	TXD=0V, R_{Load} =60Ω
			4.45	10	mA	TXD=VDD_2
Thermal-Shutdown Threshold	T_{TS}	155	165	180	℃	
Common Mode Transient Immunity	CMTI	±80	±100		kV/us	
Logic Side						
High level input voltage	V_{IH}	2			V	TXD pin
Low level input voltage	V_{IL}			0.8	V	TXD pin
High level input current	I_{IH}			10	uA	TXD pin
Low level input current	I_{IL}	-10			uA	TXD pin
Output Voltage High	V_{OH}	VDD_1-0.4			V	I_{OH} = -4mA, RXD pin

Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA, RXD pin
Input Capacitance	C_{IN}		2		pF	TXD pin
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4	V	VI=0V, R_{Load} =60Ω
CANL output voltage (Dominant)	$V_{OL(D)}$	0.8	1.33	2	V	VI=0V, R_{Load} =60Ω
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	2.5	3	V	TXD=VCC1, R_{Load} =60Ω
Differential output voltage(Dominant)	$V_{OD(D)}$	1.5		3	V	TXD=0, R_{Load} =60Ω
		1		3		TXD=0,R_{Load} =45Ω
Differential output voltage(Recessive)	$V_{OD(R)}$	-0.12		0.012	V	TXD=VCC1, R_{Load} =60 Ω , see Figure 2.1
		-0.5		0.05	V	TXD=VCC1, NO Load
Common-mode output voltage	V_{OC}	2	2.5	3	V	
Peak-to-peak Common-mode output voltage	$V_{OC(PP)}$		250		mV	
Short- circuit output current	I_{OS}	-105	-44.1		mA	CANH=-12V, CANL open, see Figure 2.10
			0.28	1	mA	CANH=12V, CANL open, see Figure 2.10
		-1	-0.44		mA	CANL=-12V, CANH open, see Figure 2.10
			42.5	105	mA	CANL=12V, CANH open, see Figure 2.10
Receiver						
Positive-going bus input threshold voltage	V_{IT+}		750	900	mV	
Negative-going bus input threshold voltage	V_{IT-}	500	650		mV	
Hysteresis voltage	V_{HYS}		100		mV	
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input	C_{ID}		5		pF	
Differential input resistance	R_{ID}	30		80	kΩ	
Input resistance	R_{IN}	15	30	40	kΩ	
Input resistance matching	RI_{match}	-3		+3	%	CANH=CANL
Common-mode voltage range	V_{COM}	-12		+12	V	

5.2. SWITCHING ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Loop delay1	T_{loop1}	100	165	210	ns	Driver input to receiver output, Recessive to Dominant
Loop delay2	T_{loop2}	80	125	170	ns	Driver input to receiver output, Dominant to Recessive
Driver						
Propagation delay time, recessive -to- dominant output	t_{PLH}		53	140	ns	
Propagation delay time, dominant -to- recessive output	t_{PHL}		78	110	ns	
Differential output signal rise time	t_r		42		ns	
Differential output signal fall time	t_f		32		ns	
Bus dominant time-out time	t_{TXD_DTO}	300	468	700	us	See Figure 2.9
Receiver						
Propagation delay time, low-to-high-level output	t_{PLH}	80	100	150	ns	
Propagation delay time, high-to-low-level output	t_{PHL}	65	80	150	ns	
RXD signal rise time	t_r		3		ns	
RXD signal fall time	t_f		3		ns	
Fail-Safe output delay time from bus-side power loss	t_{fs}		4.2		us	VDD_1=5V

5.3. PARAMETER MEASUREMENT INFORMATION

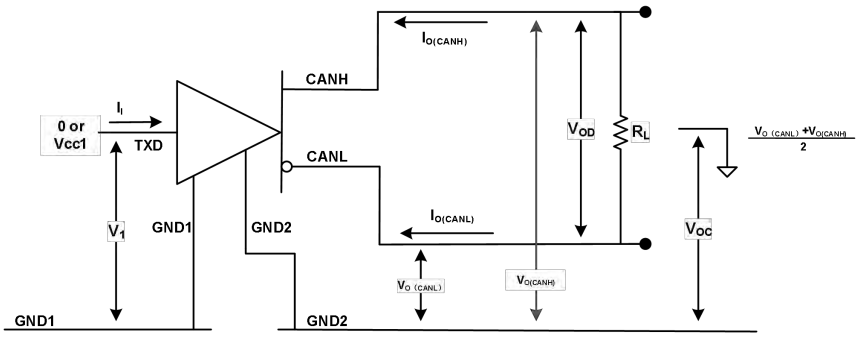


Figure 3.1. Driver Voltage, Current and Test Definitions

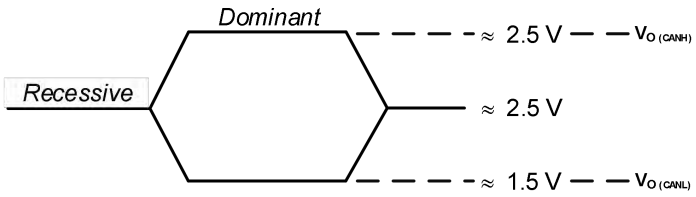


Figure 3.2. Bus Logic State Voltage Definitions

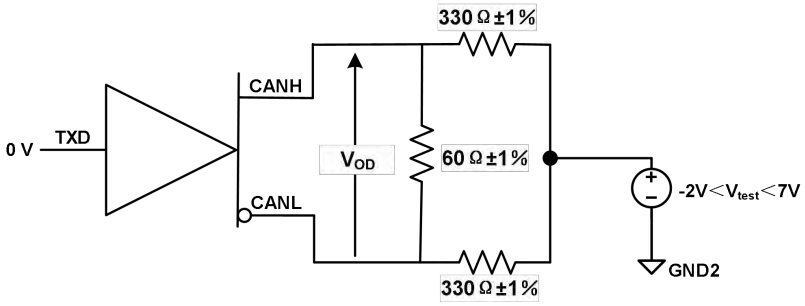
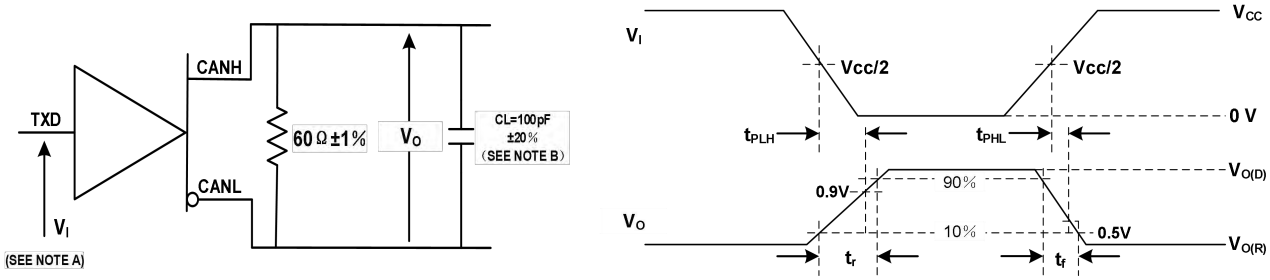


Figure 3.3. Driver VOD With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, tr ⩽ 6 ns, tf ⩽ 6 ns, ZO = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 3.4. Driver Test Circuit and Voltage Waveform

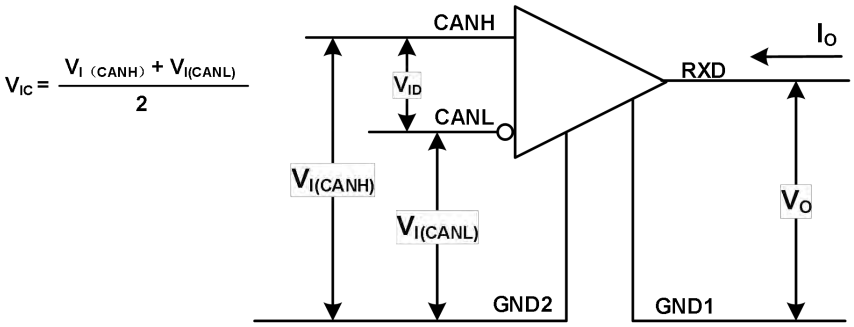
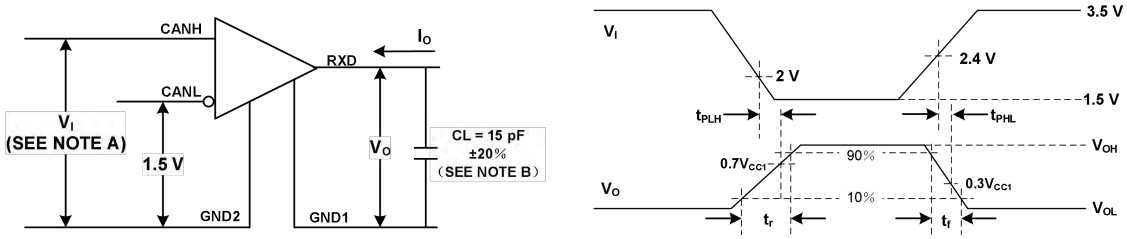


Figure 3.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 3.6. Receiver Test Circuit and Voltage Waveform

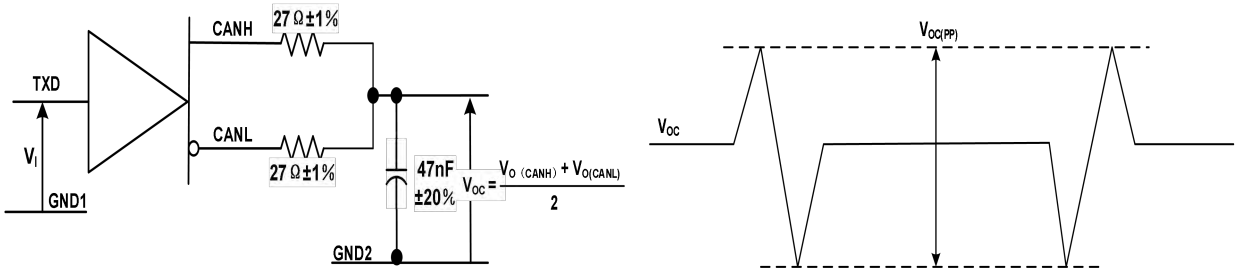


Figure 3.7. Peak-to-Peak Output Voltage Test Circuit and Waveform

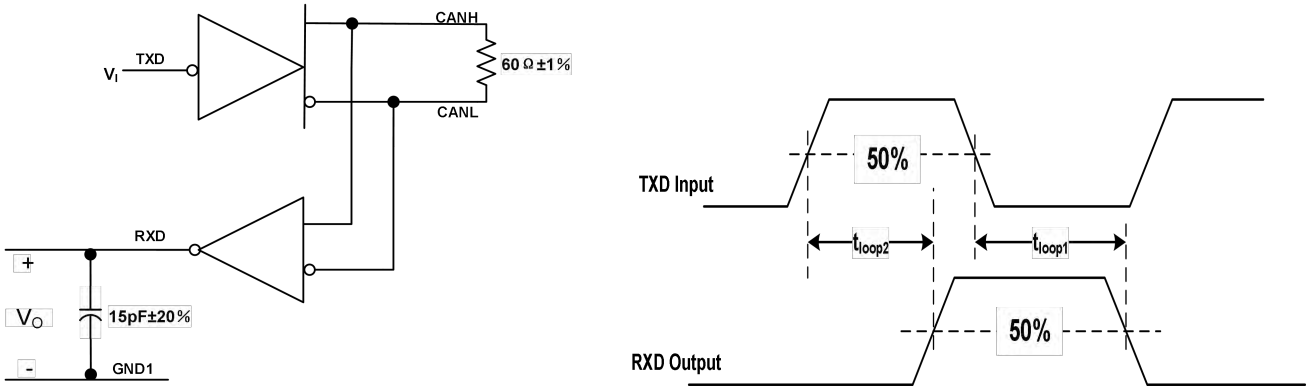
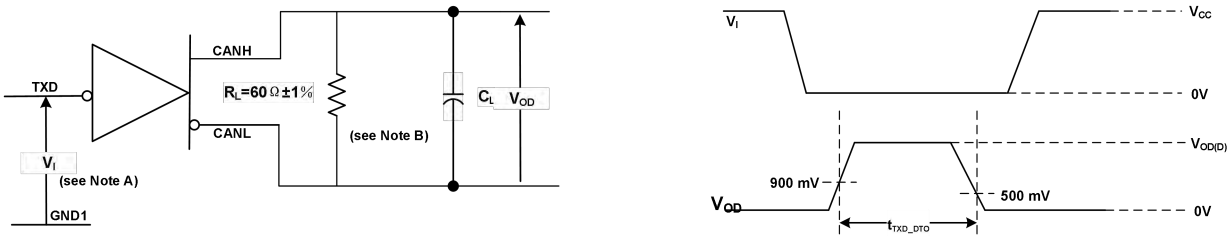


Figure 3.8. t_{LOOP} Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 3.9. Dominant Time-out Test Circuit and Voltage Waveform

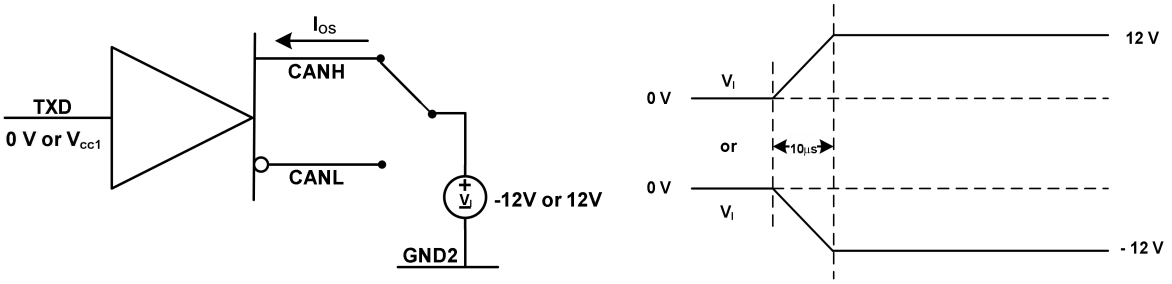


Figure 3.10. Driver Short-Circuit Current Test Circuit and Waveform

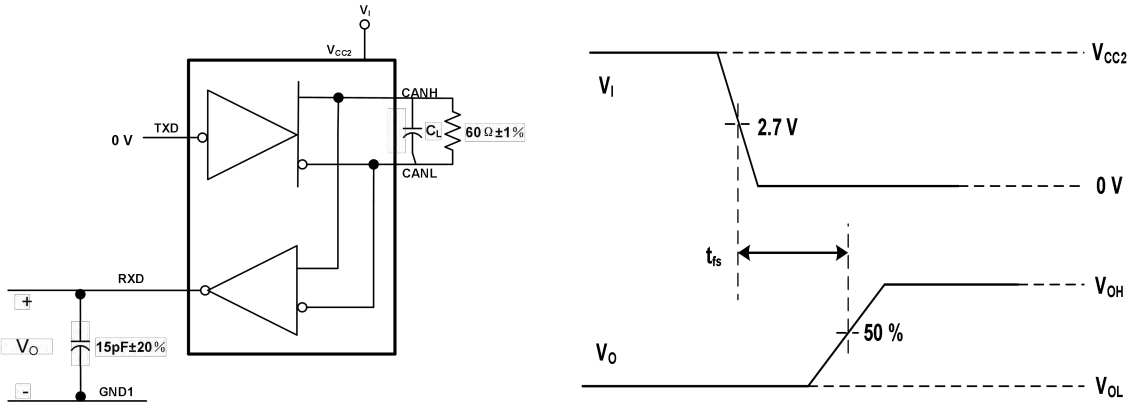


Figure 3.11. Fail-Safe Delay Time Test Circuit and Voltage Waveform

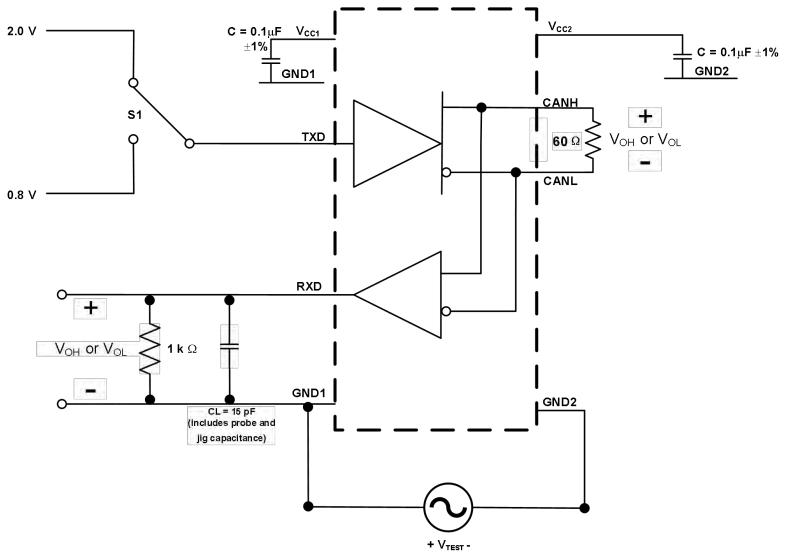


Figure 3.12. Common-Mode Transient Immunity Test Circuit

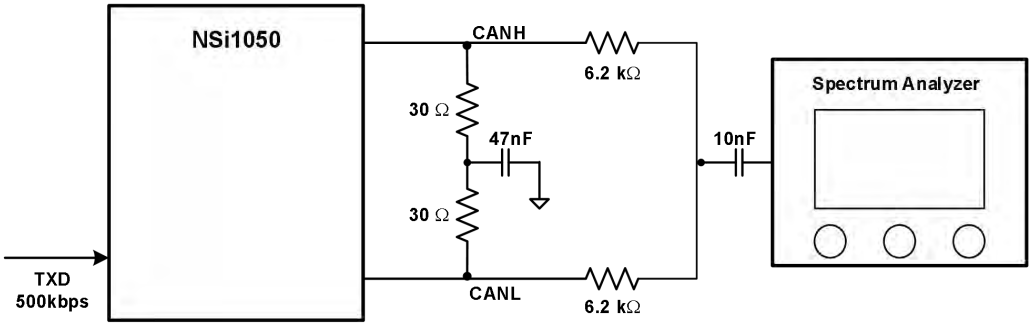


Figure 3.13. Electromagnetic Emissions Measurement Setup

6.0 HIGH VOLTAGE FEATURE DESCRIPTION

6.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	*Symbol*	*Value*		*Unit*	*Comments*
		DUB8	*SOW16*		
Minimum External Air Gap (Clearance)	L(I01)	6.5	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	6.5	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅱ	Ⅰ		

6.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 INSULATION CHARATERISTICS

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			DUB8	SOW16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150V_{rms}			Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅲ	
For Rated Mains Voltage ≤ 400V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅲ	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	1500	V_{RMS}
	DC voltage		565	2121	V_{DC}
Maximum repetitive isolation voltage		VIORM	565	2121	Vpeak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.5 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	847	/	Vpeak
	V_{IORM} × 1.875 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC		/	3977	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	V_{IORM} × 1.2= $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	/	Vpeak
	V_{IORM} × 1.2= $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	/	3394	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2= $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	2545	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	5300	8000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.3	VIOSM	5384	/	Vpeak

	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.6		/	6250	Vpeak
Isolation resistance	V_{IO} =500V at T_{amb}=T_S	RIO	>10^9	>10^9	Ω
	V_{IO} =500V at 100℃≤T_{amb}≤125℃		>10^{11}	>10^{11}	Ω
Isolation capacitance	f = 1MHz	CIO	0.8	0.8	pF
Input capacitance		CI	2	2	pF
Total Power Dissipation at 25℃		Ps	1.7	1.5	W
Safety input, output, or supply current	θJA = 72°C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	310		mA
Safety input, output, or supply current	θJA = 84 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is		299	mA
Case Temperature		Ts	150	150	℃

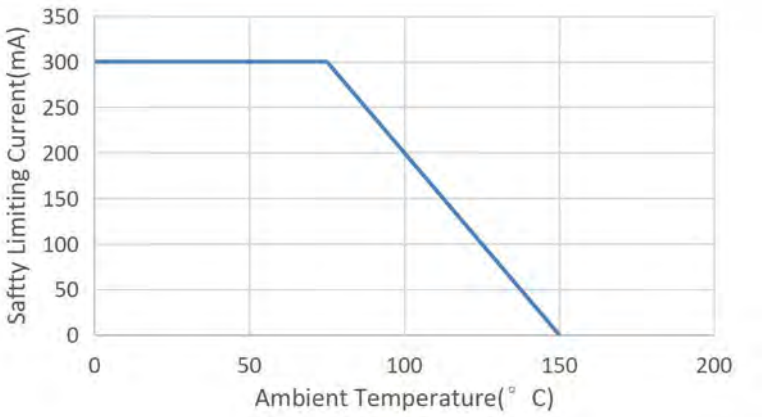


Figure 3.1 NSi1050-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

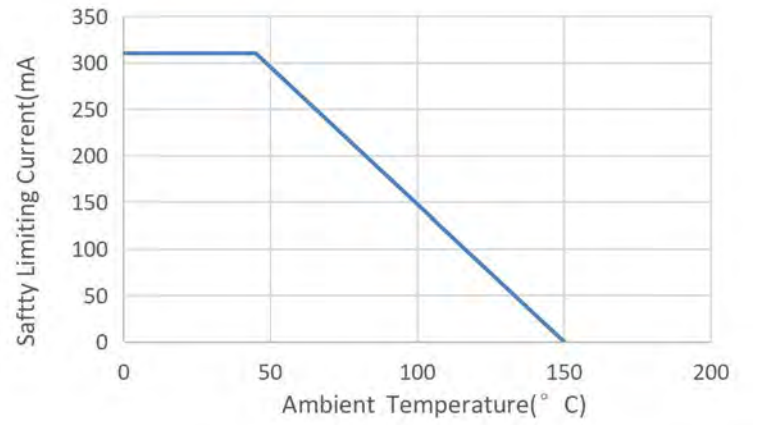


Figure 3.1 NSi1050-DDBR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. REGULATORY INFORMATION

The NSi1050-DDBR is approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation at 400V_{rms} (565Vpeak)
File (E500602)	File (E500602)	File (40050121)	File (CQC20001263786)

The NSi1050-DSWR is approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation 2121Vpeak, V_{IOSM}=6250peak	Basic insulation at 1500V_{rms} (2121Vpeak)
File (E500602)	File (E500602)	File (pending)	File (CQC20001264939)

7.0 FUNCTION DESCRIPTION

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050-DSWR device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while the NSi1050-DDBR device is safety certified by UL1577 support 3kV_{rms} insulation withstand voltages. The NSi1050 is providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps, and it can support at least 110 CAN nodes. The NSi1050 provides thermal protection and transmit data dominant time out function.

7.1. DEVICE FUNCTIONAL MODES

Table 4.1. Driver Function Table

TXD	*CANH*	*CANL*	*BUS STATE*
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to $V_{CC}/2$

Table 4.2. Receiver Function Table

V_{ID}=CANH-CANL	RXD	BUS STATE
$V_{ID} \geqslant 0.9V$	L	Dominant
$0.5< V_{ID} <0.9V$	X	Uncertain
$V_{ID} \leqslant 0.5V$	H	Recessive
Open	H	Recessive

[1] H= high level; L=low level; X= uncertain

7.2. TXD DOMINANT TIME-OUT FUNCTION

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state(blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

7.3. CURRENT PROTECTION

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

7.4. OVER TEMPERATURE PROTECTION

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

8.0 APPLICATION NOTE

8.1. TYPICAL APPLICATION

The NSi1050 requires a 0.1 µF bypass capacitors between VDD1 and GND1, VDD2and GND2. The capacitor should be placed as close as possible to the package. The figure5.1 is the basic schematic of NSi1050.

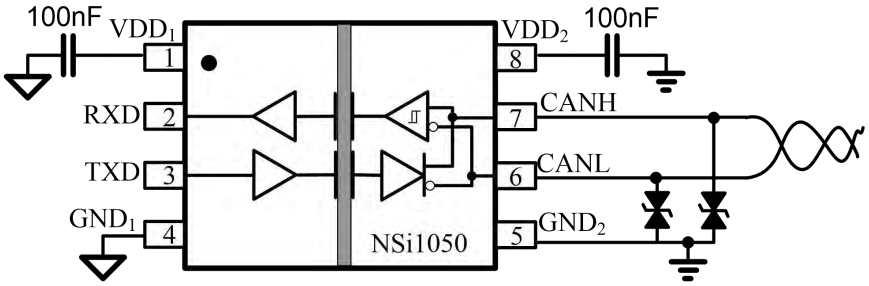


Figure6.1 Basic schematic of NSi1050

8.2. PCB LAYOUT

The recommended PCB layout shown below.

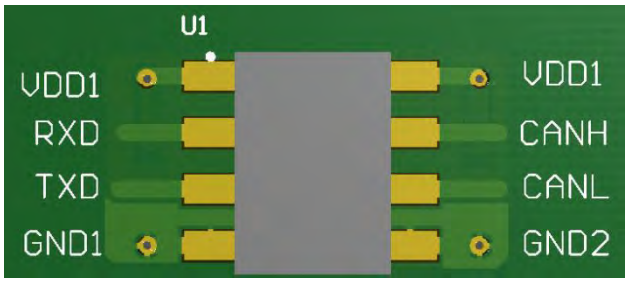
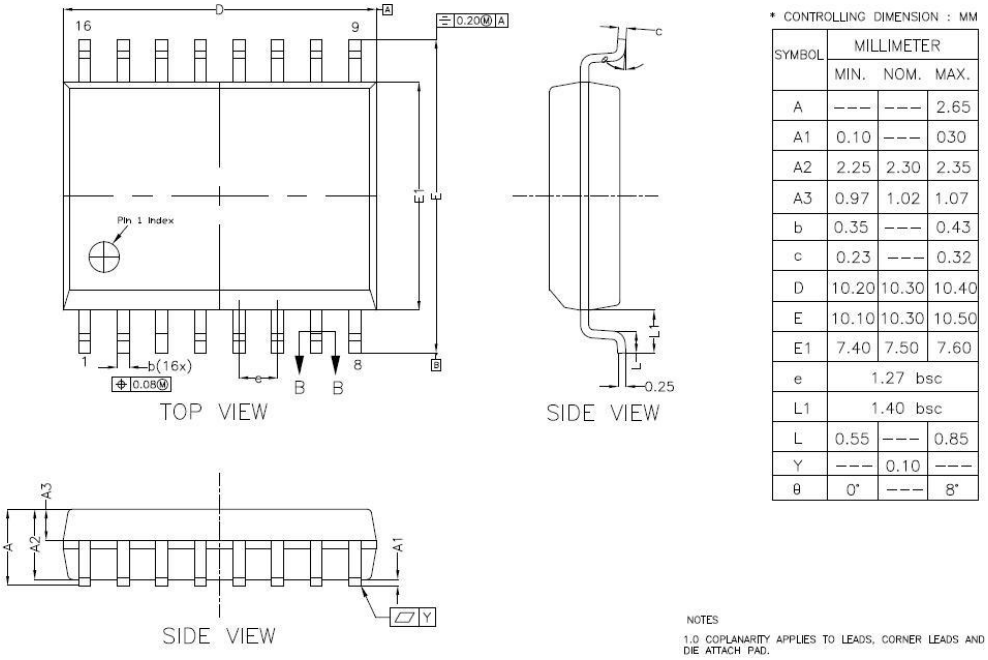


Figure6.2 Recommended PCB Layout — Top Layer

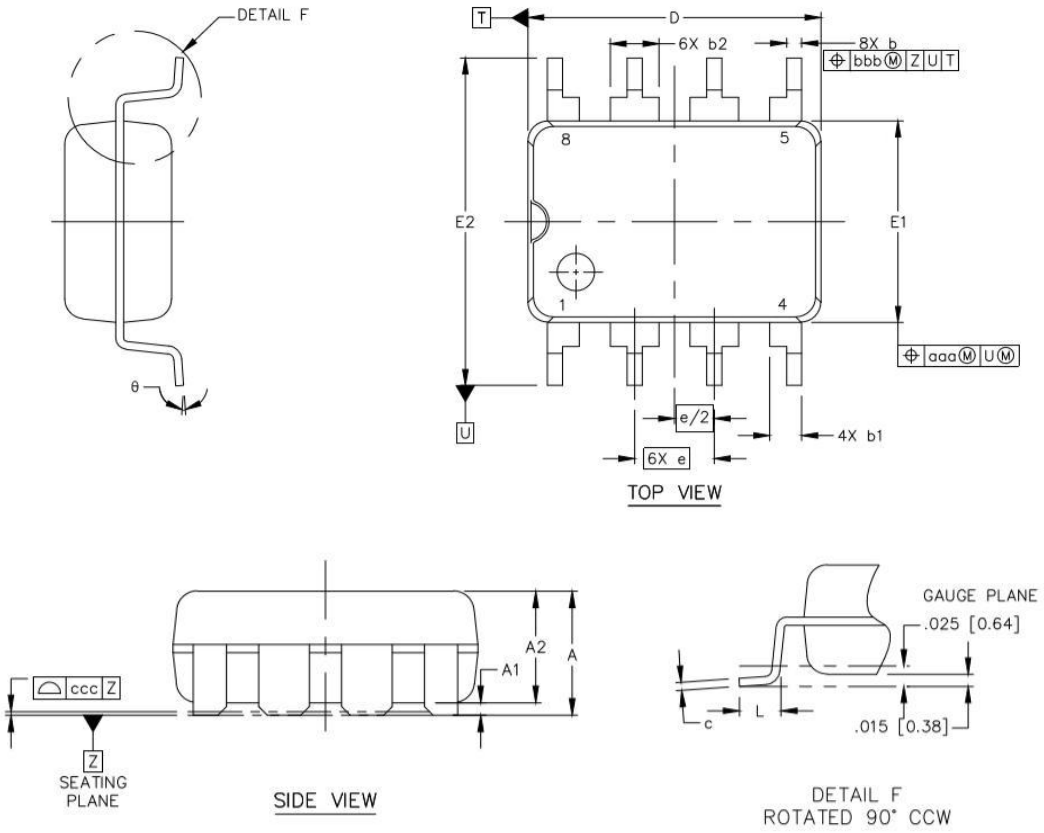
Figure6.3 Recommended PCB Layout — Bottom Layer

9.0 PACKAGE INFORMATION



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 7.1 SOW16 Package Shape and Dimension in millimeters (inches)


DETAIL F
θ
T
D
6X b2
8X b
bbb M Z U T
8
5
E2
E1
1
4
aaa M U M
U
e/2
4X b1
6X e
TOP VIEW
ccc Z
Z
SEATING
PLANE
A2
A
A1
SIDE VIEW
GAUGE PLANE
.025 [0.64]
c
L
.015 [0.38]
DETAIL F
ROTATED 90° CCW

	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.141	---	.165	3.58	---	4.19
STAND OFF	A1	.015	---	.023	0.38	---	0.58
MOLD THICKNESS	A2	.126	---	.142	3.20	---	3.61
LEAD WIDTH	b	.014	---	.022	0.36	---	0.56
	b1	---	0.039 REF	---	---	0.99 REF	---
	b2	---	0.06 REF	---	---	1.524 REF	--
L/F THICKNESS	c	.008	---	.014	0.20	---	0.36
BODY SIZE	D	.365	---	.369	9.27	---	9.37
	E1	.244	---	.260	6.20	---	6.60
	E2	.398	---	.421	10.11	---	10.69
LEAD PITCH	e	.100 BSC			2.54 BSC		
LEAD LENGTH	L	.0453	---	.0571	1.15	---	1.45
	θ	0°	---	8°	0°	---	8°
LEAD OFFSET	aaa	.010			0.254		

Figure 7.2 DUB8 Package Shape and Dimension in millimeters (inches)

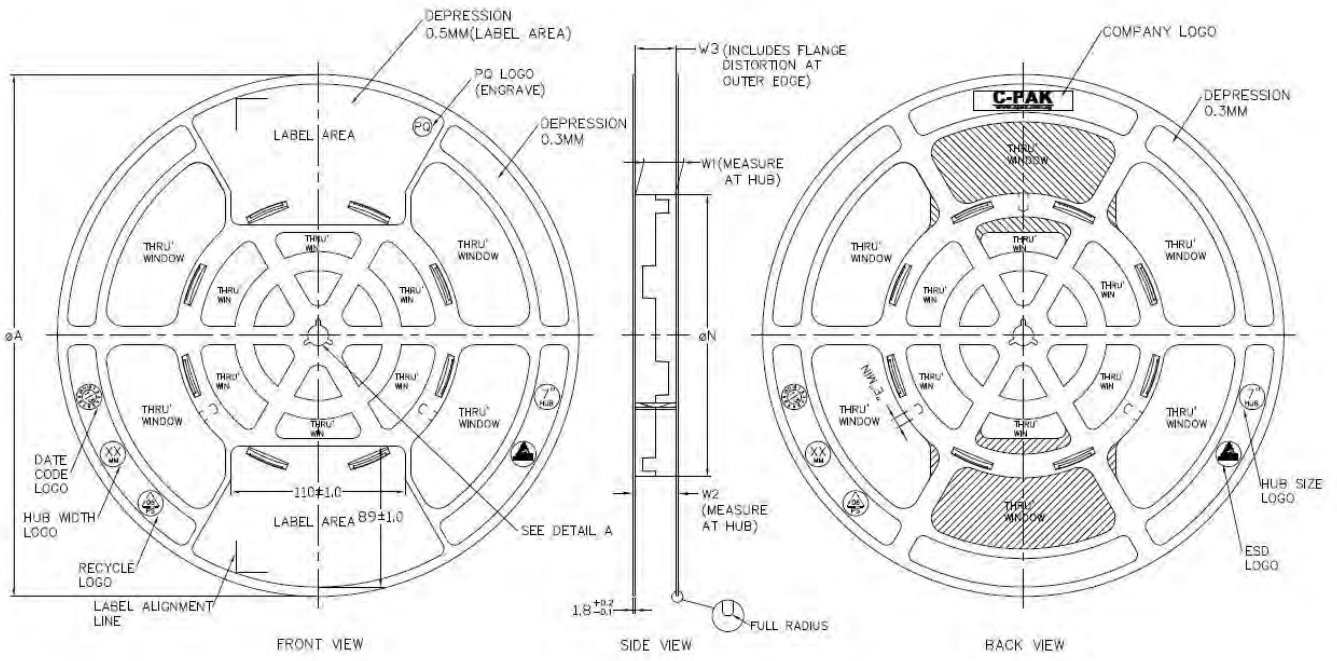
10.0 ORDER INFORMATION

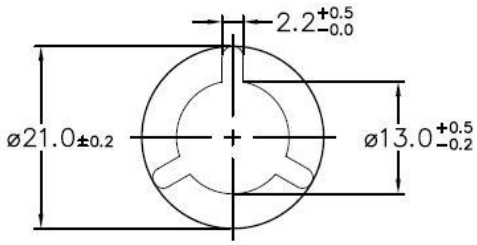
Part Number	*Isolation Rating (kV)*	*Max Data Rate (Mbps)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NSI1050-DDBR	3	1	-40 to 125℃	3	DUB8	DUB8	800
NSI1050-DSWR	5	1	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.							

11.0 DOCUMENTATION SUPPORT

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI1050	Click here	Click here	Click here	Click here

12.0 TAPE AND REEL INFORMATION

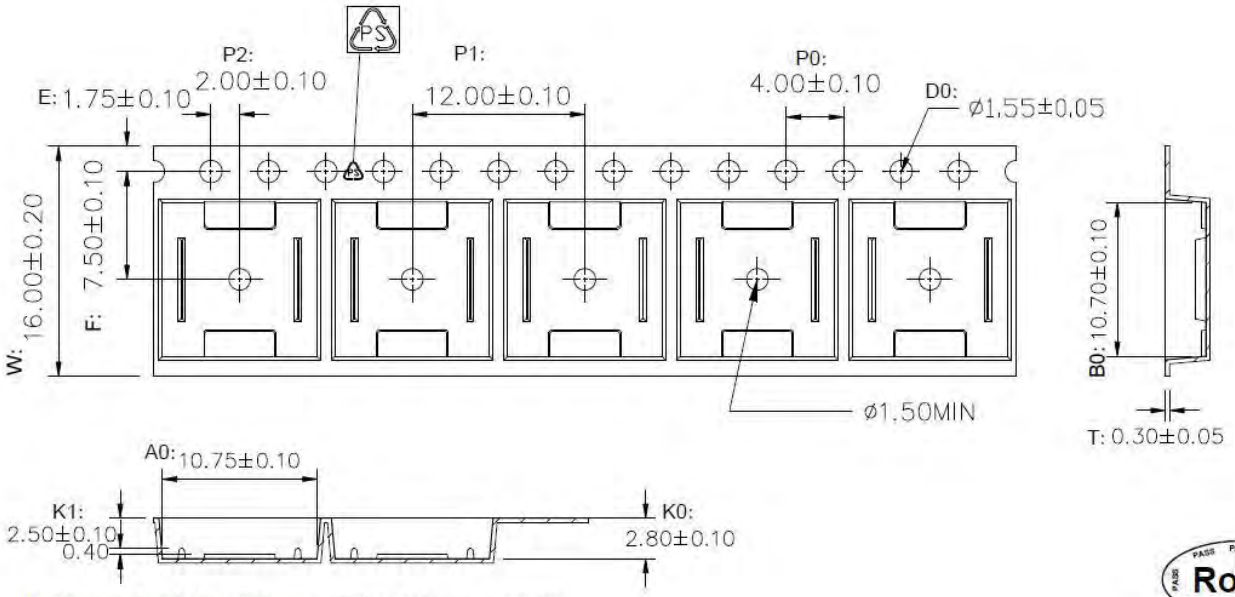




ARBOR HOLE
DETAIL A
SCALE : 3:1

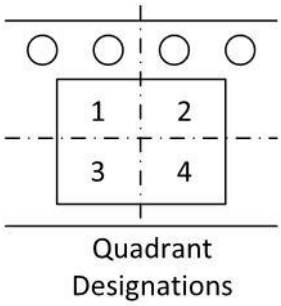
PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : 10^{5} ~ 10^{10} Ω/□

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10



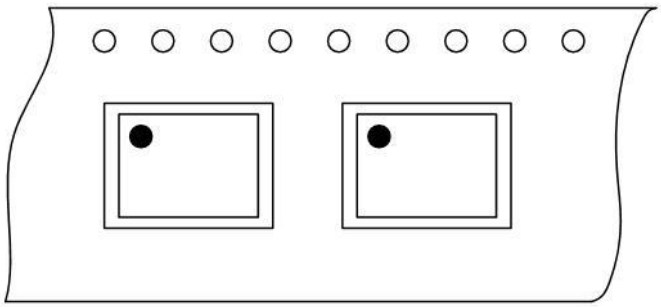
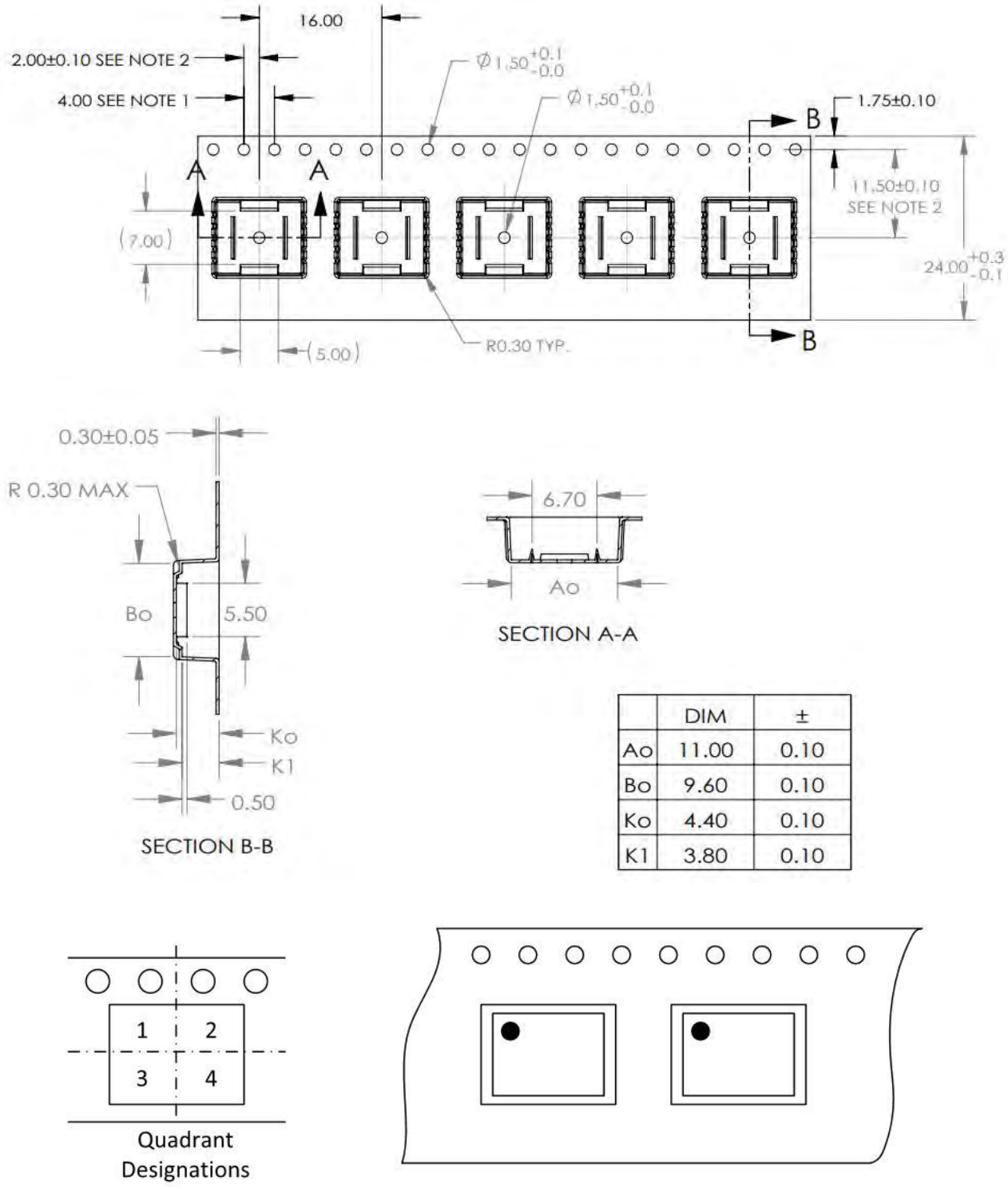


Figure 7.1 Tape and Reel Information of SOW16



	DIM	±
Ao	11.00	0.10
Bo	9.60	0.10
Ko	4.40	0.10
K1	3.80	0.10

Figure 7.2 Tape and Reel Information of DUB8

13.0 REVISION HISTORY

Revision	Description	Date
1.0	Initial version	2020/8/7

1.1	Changed tape and reel information	2020/12/20
1.2	Added DUB8 tape and reel information	2021/3/1
1.3	Update Regulatory information	2021/4/13