NSi6601

Single-Channel Isolated Gate Driver

Datasheet (EN) 1.2

Product Overview

The NSi6601 is a single-channel isolated gate driver designed to drive IGBTs, power MOSFETs and SiC MOSFETs in many applications. It provides split outputs that control the rise and fall time individually. It can source and sink 5A peak current.

The NSi6601 is available in SOP8(150 mil) or SOP8(300 mil) package, which can support 3000V_{RMS} or 5700V_{RMS} isolation per UL1577. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V, while the input-side accepts from 3.1V to 17V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

With high driving current, excellent robustness, wide supply voltage range and fast signal propagation, NSi6601 is suitable for high reliability, power density and efficiency switching power system.

Key Features

- Isolated single-channel driver
- Input side supply voltage: 3.1V to 17V
- Driver side supply voltage: up to 32V with 9V and 13 UVLO options
- 5A peak source and sink output current
- High CMTI: ±150kV/us
- 78ns typical propagation delay
- Operation ambient temperature: -40°C ~125°C
- AEC-Q100 Grade1 option
- RoHS-compliant packages:
  - SOP8(150 mil)
  - SOP8(300 mil)

Safety Regulatory Approvals

- UL recognition: 3000V_{RMS} SOP8(150 mil) and 5700V_{RMS} SOP8(300 mil) for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

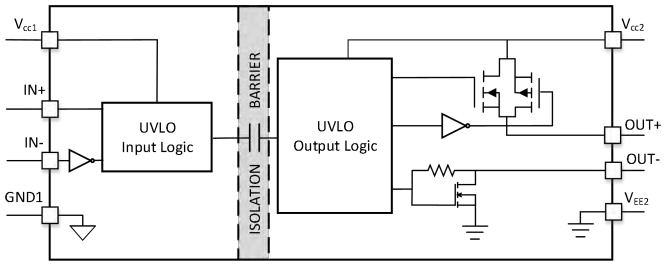
Applications

- Isolated DC/DC and AC/DC Power Supplies
- High Voltage PFC
- Solar Inverters
- Motor Drives and EV Charging
- UPS and Battery Chargers

Device Information

Part Number	*UVLO Level*	*Package*	*AEC-Q100*
NSi6601B-DSPR	9V	SOP8 (150 mil)	NO
NSi6601C-DSPR	13V	SOP8 (150 mil)	NO
NSi6601C-DSWVR	13V	SOP8 (300 mil)	NO
NSi6601B-DSWVR	9V	SOP8 (300 mil)	NO

Functional Block Diagrams



NSi6601 Block Diagram

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1. Pin Configuration and Functions

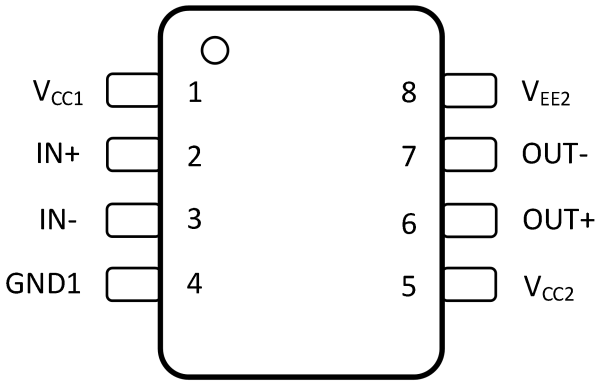


Figure 1.1 NSi6601 Top View

Table 1.1 NSi6601 Pin Configuration and Description

NSi6601 PIN NO.	*SYMBOL*	*FUNCTION*
1	V_{CC1}	Input-side supply rail
2	IN+	Non-inverted input signal with internal pull down to GND1
3	IN-	Inverted input signal with internal pull up to V_{CC1}
4	GND1	Input-side ground reference
5	V_{CC2}	Positive output supply rail
6	OUT+	Driver source output
7	OUT-	Driver sink output
8	V_{EE2}	Negative output supply rail

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Input Side Supply Voltage	V_{CC1}-GND1	-0.3	18	V
Input Signal Voltage	V_{IN+}-GND1, V_{IN-}-GND1	-0.3	18	V
Driver Side Supply Voltage	V_{CC2}-V_{EE2}	-0.3	35	V
Output Signal Voltage	V_{OUT+}, V_{OUT-}	V_{EE2}-0.3	V_{CC2}+0.3	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C
Electrostatic discharge	V_{ESD_HBM}		±2000	V
	V_{ESD_CDM}		±1500	V

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Input Side Supply Voltage	V_{CC1}-GND1	3	17	V
Input Signal Voltage	V_{IN+}-GND1, V_{IN-}-GND1	-0.3	17	V
Driver Side Supply Voltage	V_{CC2}-V_{EE2}(NSi6601B)	10	32	V
	V_{CC2}-V_{EE2}(NSi6601C)	13.7	32	
Ambient Temperature	T_A	-40	125	°C

4. Thermal Information

Parameters	*Symbol*	*NSi6601*		*Unit*
		SOP8(150 mil)	*SOP8(300 mil)*	
Junction–to-ambient thermal resistance	$R_{\theta JA}$	110	120	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	18	38	°C/W

5. Specifications

5.1. DC Electrical Characteristics

(Unless otherwise noted, V_{CC1}=5V to GND1, V_{CC2}=15V, V_{EE2}=GND2. Typical values are at T_A=25°C. All min and max specifications are at T_A=-40°C to 125°C)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Supply Currents						
Input Supply Quiescent Current	I_{CC1}		0.9	1.5	mA	
Output Supply Quiescent Current	I_{CC2}		1.6	3	mA	
Input Side Supply UVLO Threshold						
VCC1 UVLO Rising Threshold	V_{CC1_ON}		2.9	3.1	V	
VCC1 UVLO Falling Threshold	V_{CC1_OFF}	2.55	2.79		V	
VCC1 UVLO Hysteresis	V_{CC1_HYS}		0.11		V	
Driver Side Supply UVLO Threshold (NSi6601B, 9V UVLO Level)						
VCC2 UVLO Rising Threshold	V_{CC2_ON}		9.2	10	V	
VCC2 UVLO Falling Threshold	V_{CC2_OFF}	8	8.5		V	
VCC2 UVLO Hysteresis	V_{CC2_HYS}		0.7		V	
Driver Side Supply UVLO Threshold (NSi6601C, 13V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC_ON}		13.2	13.7	V	
VCC UVLO Falling Threshold	V_{CC_OFF}	11.7	12.3		V	
VCC UVLO Hysteresis	V_{CC_HYS}		0.9		V	
Input Pin Characteristic						
Logic High Input Threshold (IN+, IN-)	V_{IN+H}, V_{IN-H}			0.7×V_{CC1}	V	
Logic Low Input Threshold (IN+, IN-)	V_{IN+L}, V_{IN-L}	0.3×V_{CC1}			V	
Input Hysteresis Voltage (IN+, IN-)	V_{hys_IN}		0.1×V_{CC1}		V	
IN+ Input Current	I_{IN+}		55	100	uA	V_{IN+}=V_{CC1}
IN- Input Current	I_{IN-}		55	100	uA	V_{IN-}=GND1
Output Pin Characteristic						
High Level Output Voltage	V_{OH}	V_{CC2}-0.25	V_{CC2}-0.14		V	I_{OUT+}=-50mA, V_{IN+}=High, V_{IN-}=Low
Low Level Output Voltage	V_{OL}		30	60	mV	I_{OUT-}=50mA, V_{IN+}=Low, V_{IN-}=High
Peak Source Output Current	I_{OUT+}	4	5		A	V_{CC2}=15V, pulse width<10us
Peak Sink Output Current	I_{OUT-}	4	5		A	V_{CC2}=15V, pulse width<10us

5.2. Switching Characteristics

(Unless otherwise noted, V_{CC1}=5V to GND1, V_{CC2}=15V, V_{EE2}=GND2. Typical values are at T_A=25°C. All min and max specifications are at T_A=-40°C to 125°C)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Minimum Pulse Width	t_{PWmin}		30	70	ns	
Propagation Delay	t_{pLH}	50	78	110	ns	C_{LOAD}=100pF
Propagation Delay	t_{pHL}	50	78	110	ns	C_{LOAD}=100pF
Pulse Width Distortion $\|t_{PLH}-t_{PHL}\|$	t_{PWD}		2	25	ns	C_{LOAD}=100pF
Output Rise Time (20% to 80%)	t_R		9	20	ns	C_{LOAD}=1nF
Output Fall Time (80% to 20%)	t_F		8	19	ns	C_{LOAD}=1nF
Common Mode Transient Immunity	CMTI	150			kV/us	

5.3. Typical Performance Characteristics

(Unless otherwise noted, V_{CC1}=5V to GND1, V_{CC2}=15V, V_{EE2}=GND2, T_A=25°C)

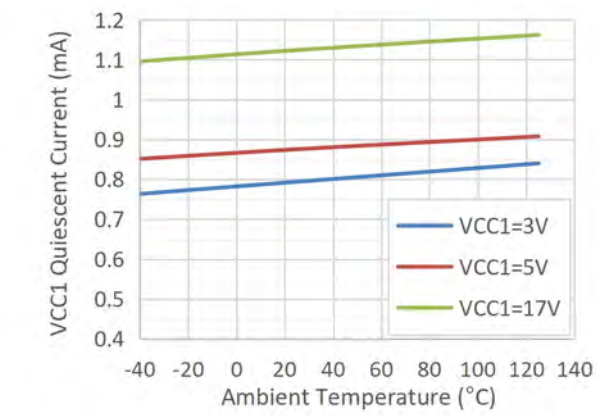


Figure 5.1 Input supply quiescent current versus Temperature

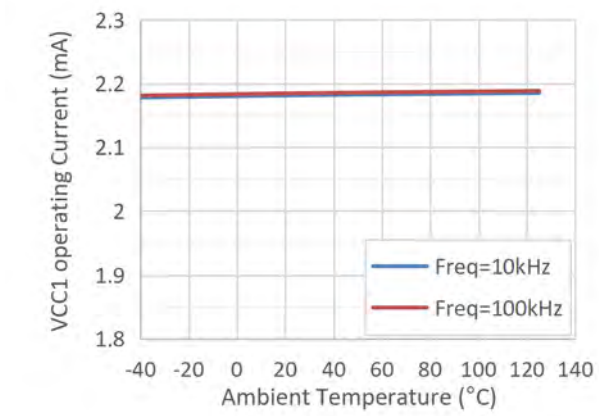


Figure 5.2 Input supply operating current versus Temperature

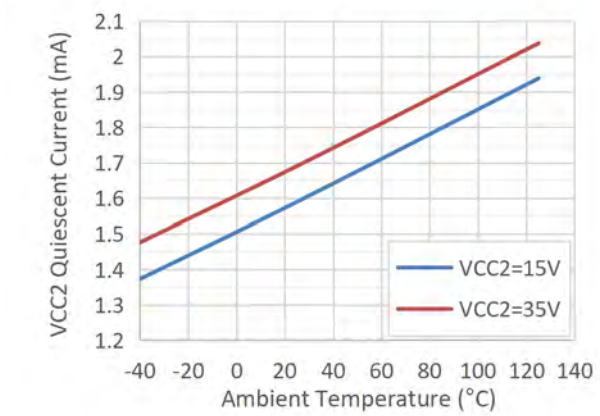


Figure 5.3 Output supply quiescent current versus Temperature

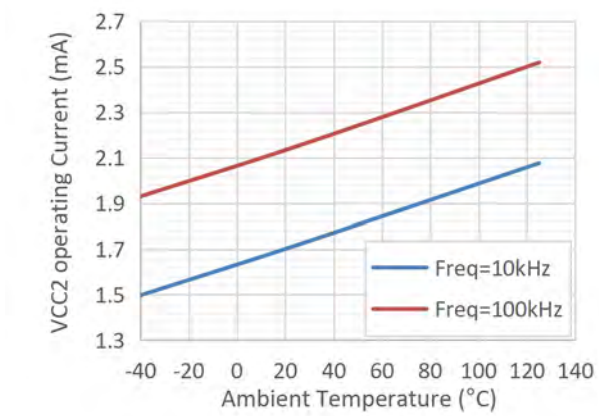


Figure 5.4 Output supply operating current versus Temperature

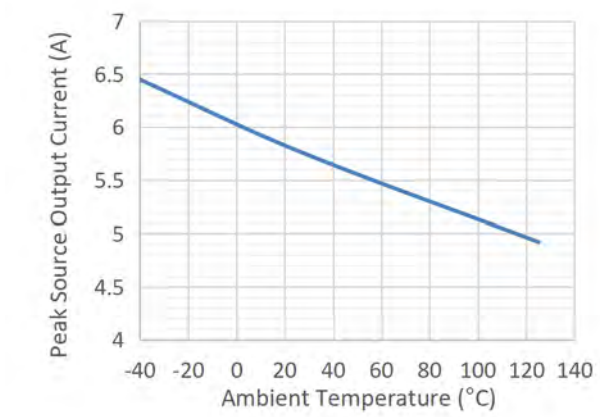


Figure 5.5 Peak source output current versus Temperature

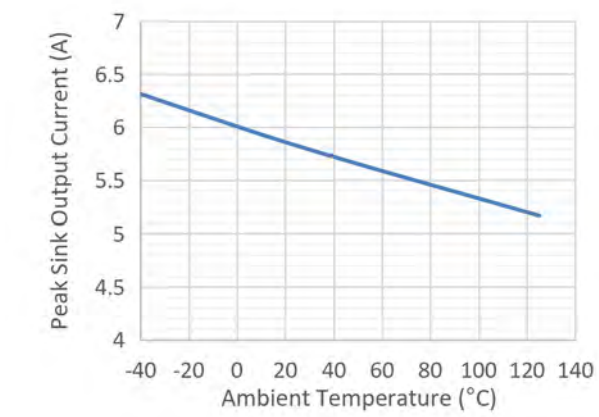


Figure 5.6 Peak sink output current versus Temperature

5.4. Parameter Measurement Information

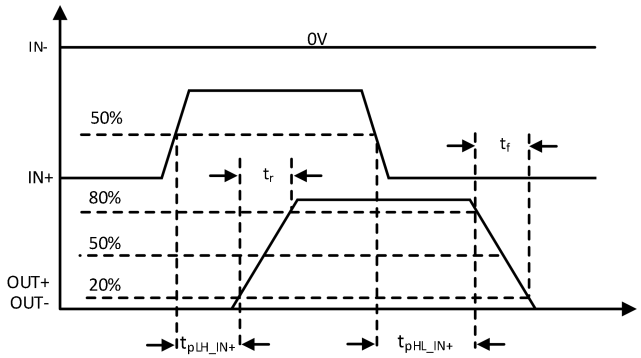


Figure 5.12 Propagation Delay, Rise Time and Fall Time, Non-inverting Configuration

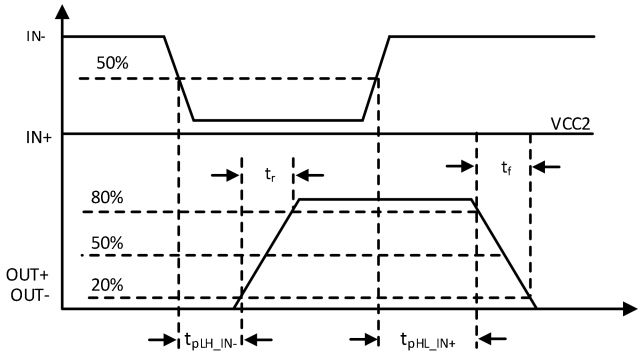


Figure 5.13 Propagation Delay, Rise Time and Fall Time, Inverting Configuration

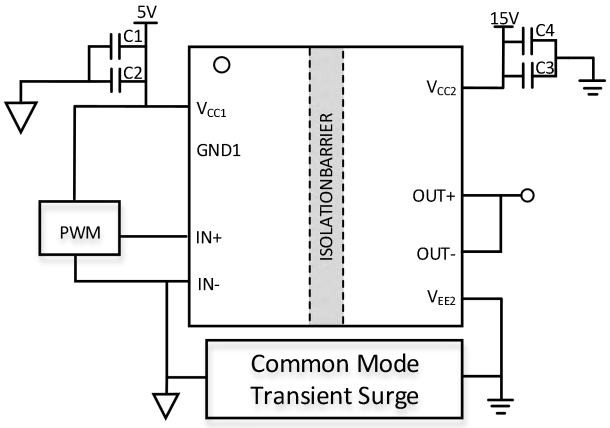


Figure 5.14 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*NSi6601*		*Unit*	*Comments*
		SOP8(150 mil)	*SOP8(300 mil)*		
Minimum External Air Gap (Clearance)	CLR	4.0	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	4.0	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20	20	um	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I	I		

6.2. DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 Insulation Characteristics for SOP8(150 mil) Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V_{RMS}			I to IV	
For Rated Mains Voltage ≤ 300 V_{RMS}			I to III	
Climatic Category			40/125/21	
Pollution Degree			2	
Maximum Working Isolation Voltage		V_{IOWM}	700	V_{RMS}
			990	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	990	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{pd(m)}$=V_{IORM}×1.5, 100% production test, t_{ini}=t_m=1s, partial discharge<5pC	$V_{pd(m)}$	1485	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	1188	V_{PEAK}
After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	1188	V_{PEAK}
Maximum Transient Isolation Voltage	t = 60 s	V_{IOTM}	4242	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{TEST}= V_{ISO}, t = 60 s (qualification); V_{TEST}= 1.2 ×V_{ISO}, t = 1 s (100%production)	V_{ISO}	3000	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, V_{TEST}=V_{IOSM}×1.3	V_{IOSM}	4242	V_{PEAK}
Isolation Resistance	V_{IO} =500V at T_A=T_S=150°C	R_{IO}	>10^9	Ω
	V_{IO} =500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF

6.3. Safety Limiting Values for SOP8(150 mil) Package

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=110°C/W, T_J=150°C, T_A=25°C	P_S	Total	1.14	W
			Input Side	0.05	
			Output Side	1.09	
Maximum Safety Current	$R_{\theta JA}$=110°C/W, V_{CC2}=15V, T_J=150°C, T_A=25°C	I_S	Output Side	73	mA
	$R_{\theta JA}$=110°C/W, V_{CC2}=30V, T_J=150°C, T_A=25°C		Output Side	36	

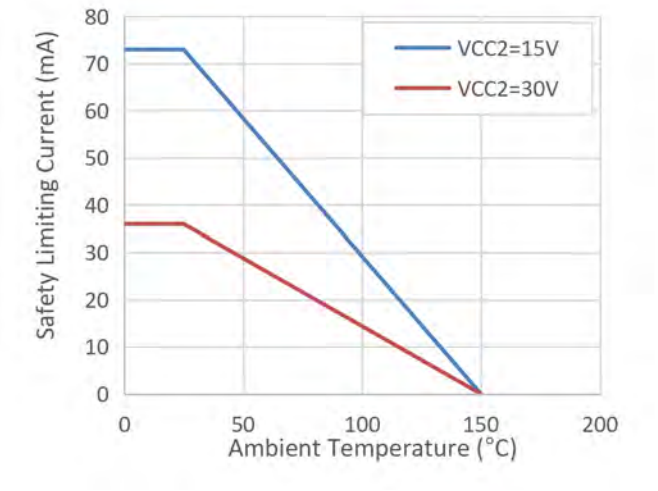


Figure 6.1 Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11 for SOP8(150 mil) Package

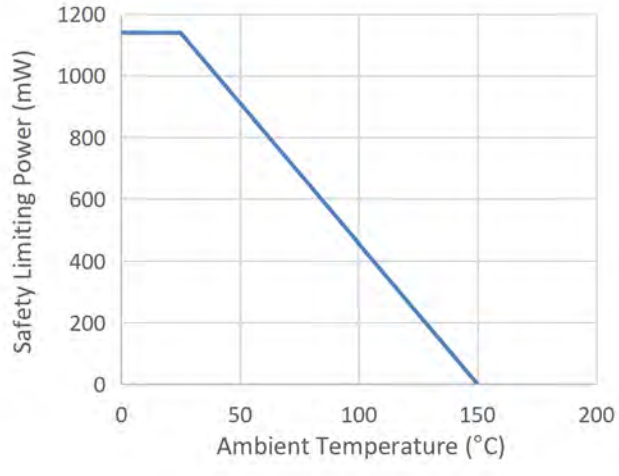


Figure 6.2 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOP8(150 mil) Package

6.4. Regulatory Information for SOP8(150 mil) Package

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, $3000V_{RMS}$ Isolation Voltage	Single Protection, $3000V_{RMS}$ Isolation voltage	Basic Insulation $V_{IORM}=990V_{PEAK}$, $V_{IOTM}=4242V_{PEAK}$, $V_{IOSM}=4242V_{PEAK}$	Basic Insulation at $700V_{RMS}$ ($990V_{PEAK}$)
E500602	File (pending)	File (pending)	CQC20001264940

6.5. DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 Insulation Characteristics for SOP8(300 mil) Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 600V_{RMS}			I to III	
For Rated Mains Voltage ≤ 1000V_{RMS}			I to II	
Climatic Category			40/125/21	
Pollution Degree			2	
Maximum Working Isolation Voltage		V_{IOWM}	1500	V_{RMS}
			2121	V_{DC}
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{pd(m)}$=V_{IORM}×1.875, 100% production test, t_{ini}=t_m=1s, partial discharge<5pC	$V_{pd(m)}$	3977	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{pd(m)}$=V_{IORM}×1.6, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	3394	V_{PEAK}
After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC	$V_{pd(m)}$	2545	V_{PEAK}
Maximum Transient Isolation Voltage	t = 60 s	V_{IOTM}	8000	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{TEST}= V_{ISO}, t = 60 s (qualification); V_{TEST}= 1.2 ×V_{ISO}, t = 1 s (100%production)	V_{ISO}	5700	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, V_{TEST}=V_{IOSM}×1.6	V_{IOSM}	6250	V_{PEAK}
Isolation Resistance	V_{IO} =500V at T_A=T_S=150°C	R_{IO}	>10^9	Ω
	V_{IO} =500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF

6.6. Safety Limiting Values for SOP8(300 mil) Package

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=120°C/W, T_J=150°C, T_A=25°C	P_S	Total	1.04	W
			Input Side	0.05	
			Output Side	0.99	
Maximum Safety Current	$R_{\theta JA}$=120°C/W, V_{CC2}=15V, T_J=150°C, T_A=25°C	I_S	Output Side	66	mA
	$R_{\theta JA}$=120°C/W, V_{CC2}=30V, T_J=150°C, T_A=25°C		Output Side	33	

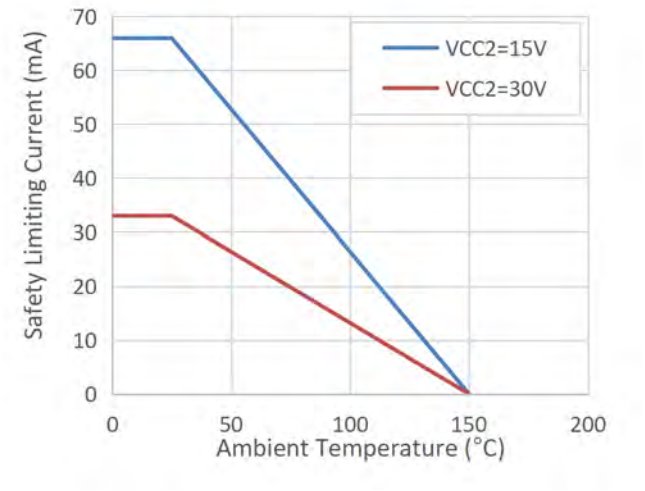


Figure 6.3 Thermal Derating Curve for Limiting Current per DIN VDE V 0884-11 for SOP8(300 mil) Package

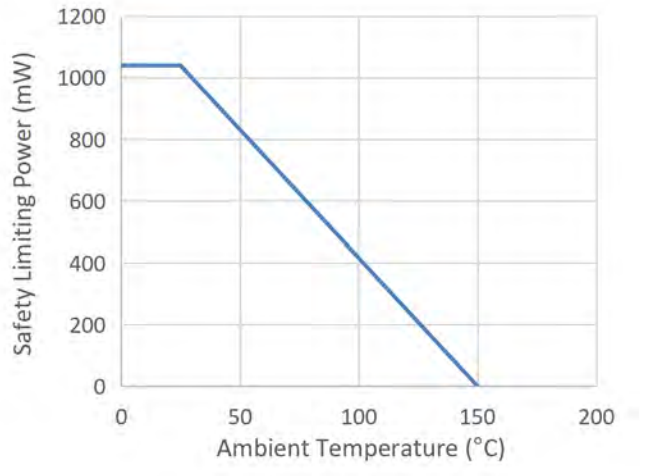


Figure 6.4 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOP8(300 mil) Package

6.7. Regulatory Information for SOP8(300 mil) Package

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5700V_{RMS} Isolation Voltage	Single Protection, 5700V_{RMS} Isolation voltage	Reinforced Insulation V_{IORM}=2121V_{PEAK}, V_{IOTM}=8000V_{PEAK}, V_{IOSM}=6250V_{PEAK}	Reinforced Insulation
File (pending)	File (pending)	File (pending)	File (pending)

7. Function Description

7.1. Overview

The NSi6601 is a high reliable power transistor gate driver. It has 9V and 13V UVLO version, which is suitable to drive MOSFET, IGBT, or SiC MOSFET. The NSi6601 is available in SOP8 narrow body or wide body package, which can support 3000V_{RMS} or 5700V_{RMS} isolation per UL1577. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The isolation barrier inside NSi6601 is based on a capacitive isolation. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI. As shown in Figure 7.2, the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The functional block diagram of NSi6601 is shown in Figure 7.1. Two Input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs can control the rise and fall time individually. Active pull-down and short circuit clamping features are implemented to protect power transistor.

7.2. Functional Block Diagram

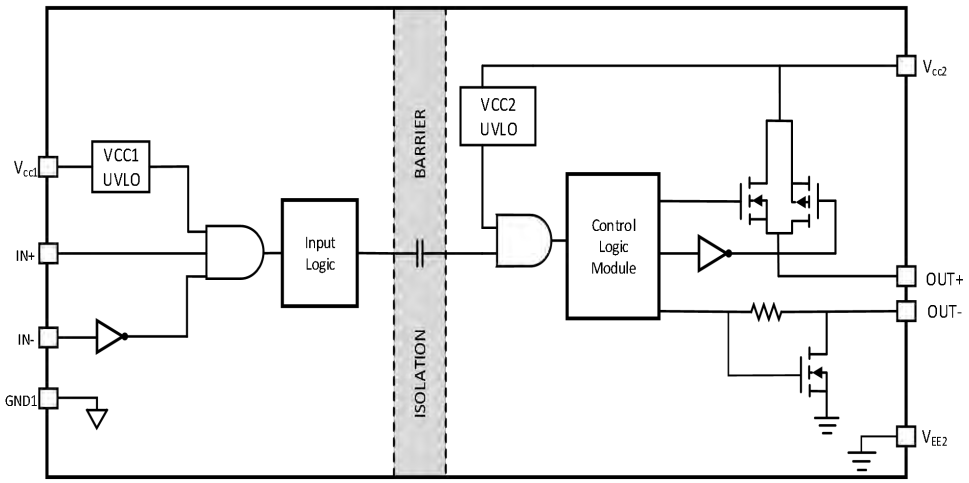


Figure 7.1 NSi6601 Functional Block Diagram

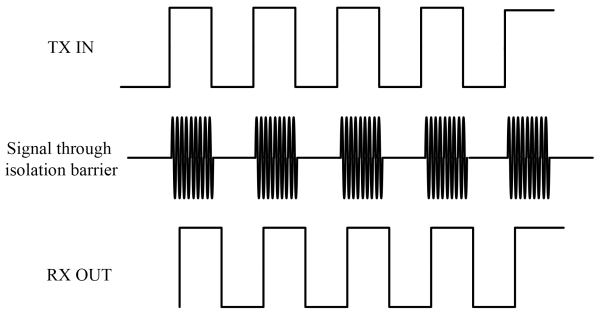


Figure 7.2 OOK Modulation

7.3. Truth Tables

Table 7.1 Driver Function Table (1)

V_{CC1} status	V_{CC2} status	Inputs		Outputs		Comment
		IN+	IN-	OUT+	OUT-	
PU	PU	H	L	H	Hi-Z	
PU	PU	L	H	Hi-Z	L	
PU	PU	H	H	Hi-Z	L	Interlock protection
PU	PU	L	L	Hi-Z	L	
PD	PU	X	X	Hi-Z	L	
PU	PD	X	X	Hi-Z	L	Active pull-down
PD	PD	X	X	Hi-Z	L	Active pull-down

(1) PD = Powered Down; PU = Powered Up; H = Logic High; L= Logic Low; X= Irrelevant

The IN+ pin is internally pulled down to GND1, while IN- pin is internally pulled up to VCC1, making the output of NSi6601 is low by default. To improve noise immunity, grounding an input or tying to VCC1 is recommended.

To control the output during normal operation, PWM from MCU is connected to IN+ pin or IN- pin. A minimum input pulse width is defined to filter occasional glitches.

From the truth table, interlock protection and active pull-down is obtained. See Chapter 7.6 and Chapter 8.2 for detailed description.

7.4. Output Stage

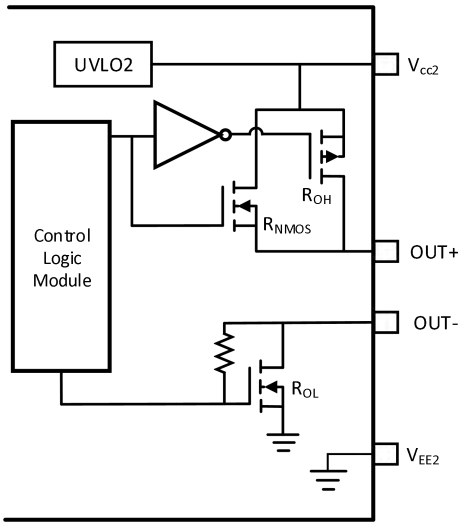


Figure 7.3 NSi6601 Output Stage

Table 7.2 NSi6601 Output Stage On-Resistance

R_{NMOS}	R_{OH}	R_{OL}	Unit
0.8	2.8	0.6	Ω

The NSi6601 has P-channel and N-channel MOSFET in parallel to pull up the OUT+ pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSi6601 N-channel MOSFET turns on to pull up OUT+ more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSi6601. The equivalent pull-up resistance of NSi6601 is the parallel combination ROH || RNMOS. The result is quite small, indicating the strong driving capability of NSi6601.The pull-down structure of NSi6601 is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSi6601.

7.5. V_{CC1}, V_{CC2} and Under Voltage Lock Out (UVLO)

To ensure correct switching the device is equipped with an undervoltage lockout for input and output power supply independently. V_{CC1} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver output can become clamped low. Output supply UVLO is referred to V_{EE2} pin. If V_{CC2}-V_{EE2} falls below the UVLO threshold, OUT- of the gate-driver will be clamped low.

Local bypass capacitors should be placed between the V_{CC2} and V_{EE2} pins, as well as the V_{CC1} and GND1 pins. 220-nF to 10-µF is recommended for device biasing. Additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. The capacitors should be positioned as close to the device as possible for better noise filtering. Low-ESR, ceramic surface-mount capacitors are recommended.

7.6. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC2} is not connected to the power supply. When V_{CC} is floating, the driver output is held low and clamping OUT to approximately 1.8V higher than V_{EE2}.

7.7. Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the miller capacitance. The diode between OUT+ and V_{CC2} pins inside the driver limits this voltage to approximately 0.7V higher than the supply voltage. A maximum current of 500mA may be fed back to the supply through this path for 10µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

8. Application Note

8.1. Typical Application Circuit

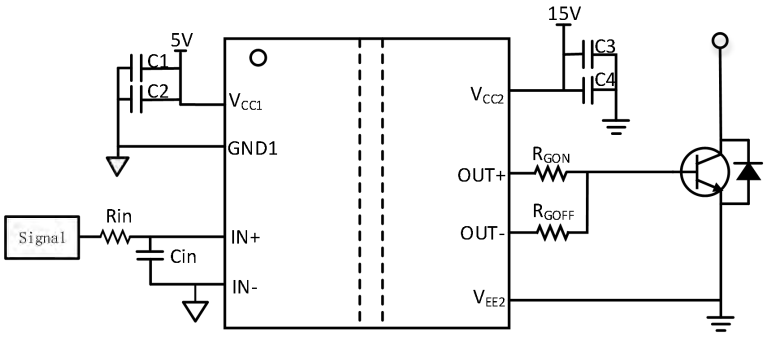


Figure 8.1 NSi6601 Typical Application Circuit

Bypassing capacitors for V_{CC1} and V_{CC2} supplies are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to place as close as possible to NSi6601, both at V_{CC1} and V_{CC2} side. For V_{CC2} supply, additional 10μF/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the V_{CC1} or V_{CC2} power supply is located long distance from the IC, bigger capacitance is needed.

The input filter composed by Rin and Cin can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

8.2. Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSi6601 can be used. Interlock protection is possible as shown in Figure 8.2. If the controller has some mistake, leading to negative dead time, the output PWM of NSi6601 is adjusted to avoid power transistor shoot through.

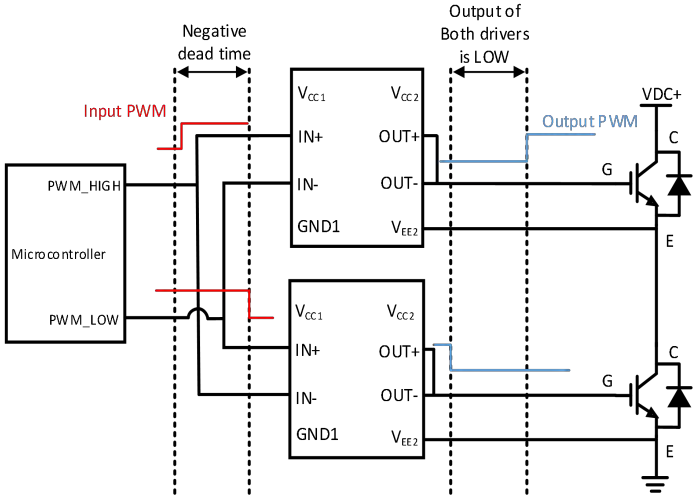


Figure 8.2 Interlock Protection using NSi6601

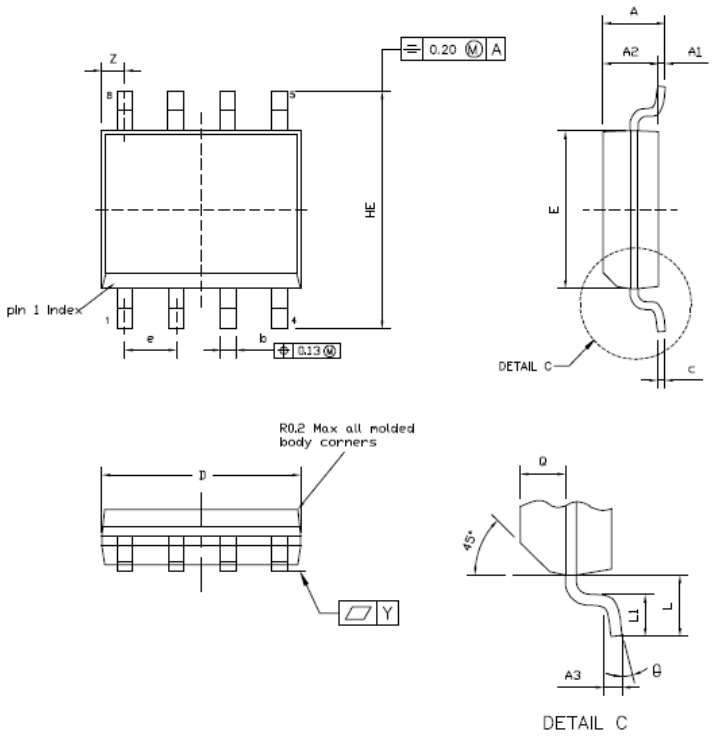
8.3. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSi6601, between V_{CC1} to GND1, or V_{CC2} to V_{EE2}.

- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSi6601 close to power transistor.
- Place large amount of copper connecting to V_{EE2} pin and V_{CC2} pin for thermal dissipation, with priority on V_{EE2} pin. If the system has multi V_{EE2} or V_{CC2} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

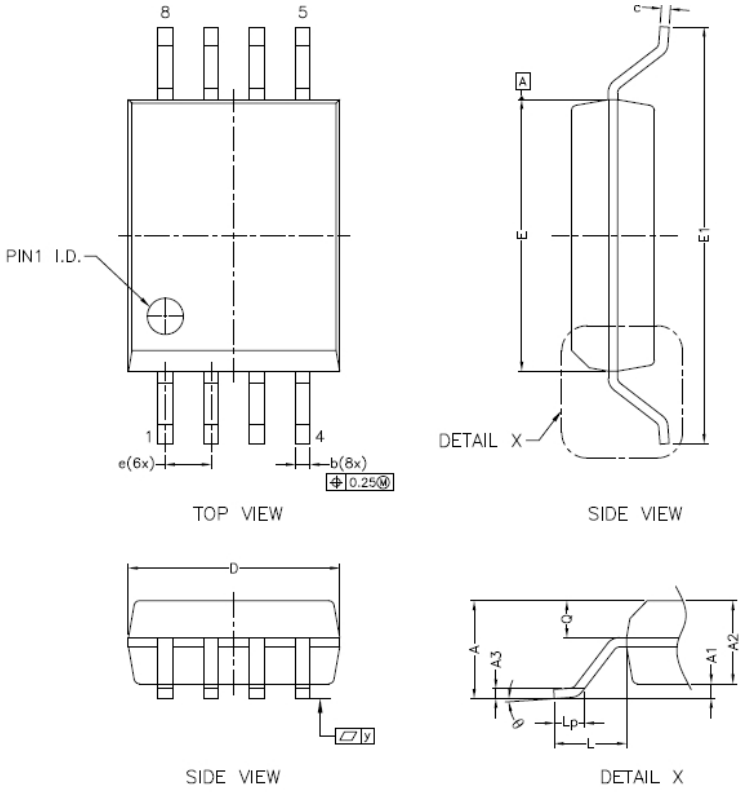
9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 9.1 SOP8(150 mil) Package Shape and Dimension in millimeters (inches)



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.2 SOP8(300 mil) Package Shape and Dimension in millimeters and (inches)

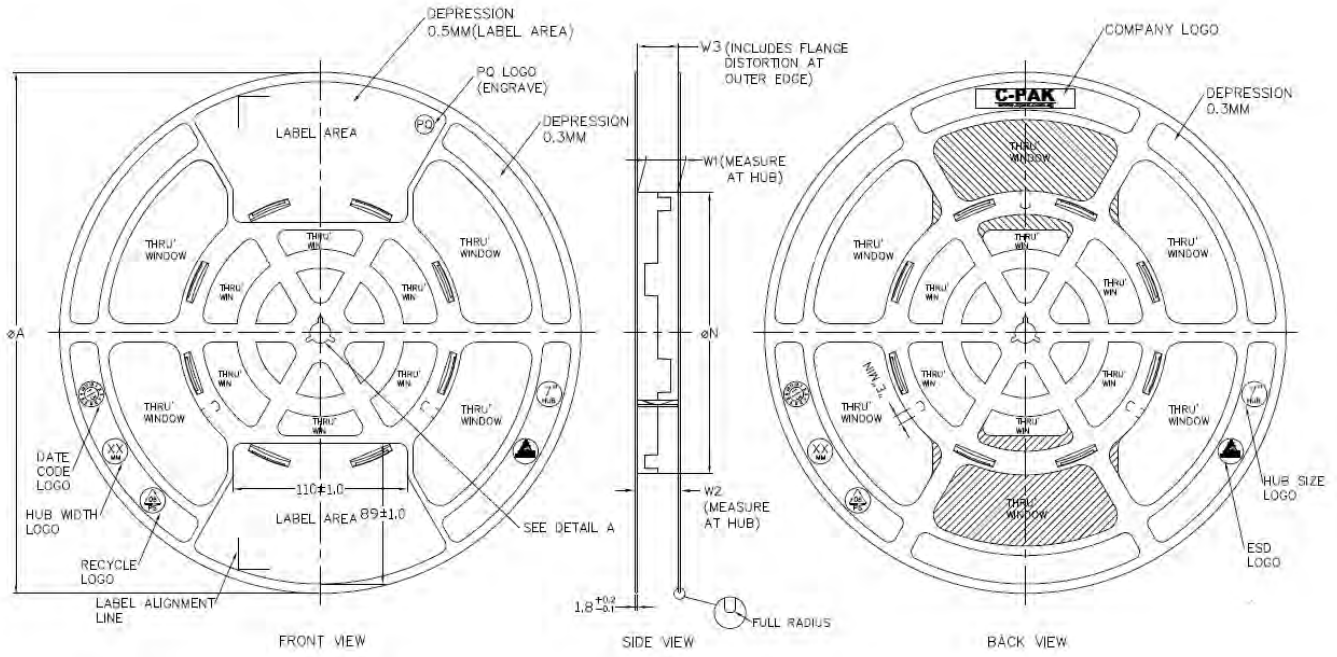
10. Ordering Information

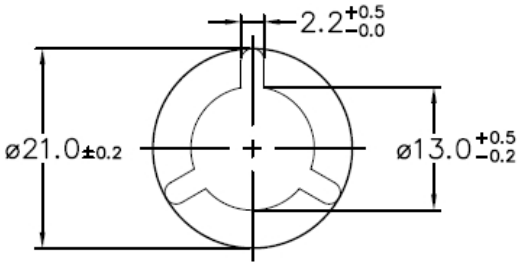
Part Number	*Isolation Rating (kV)*	*UVLO Level*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*	*AEC-Q100*
NSi6601B-DSPR	3	9V	-40 to 125°C	1	SOP8(150 mil)	SOP8	2500	NO
NSi6601C-DSPR	3	13V	-40 to 125°C	1	SOP8(150 mil)	SOP8	2500	NO
NSi6601C-DSWVR	5	13V	-40 to 125°C	3	SOP8(300 mil)	SOW8	1000	NO
NSi6601B-DSWVR	5	9V	-40 to 125°C	3	SOP8(300 mil)	SOW8	1000	NO

11. Documentation Support

Part Number	***Product Folder***	***Datasheet***	***Technical Documents***	***Isolated Driver Selection Guide***
NSi6601	Click here	Click here	Click here	Click here

12. Tape and Reel Information

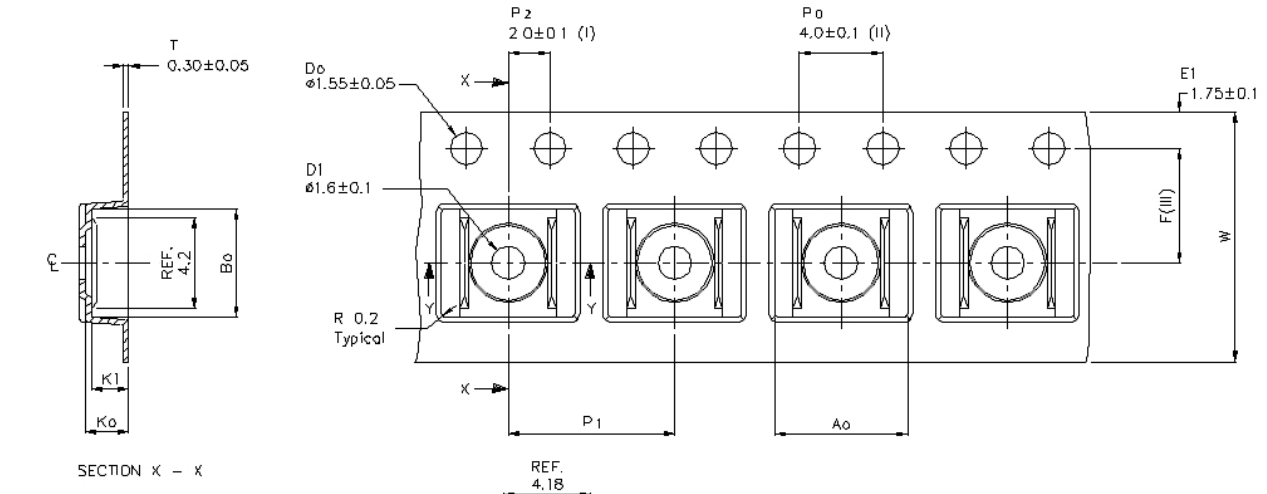




PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

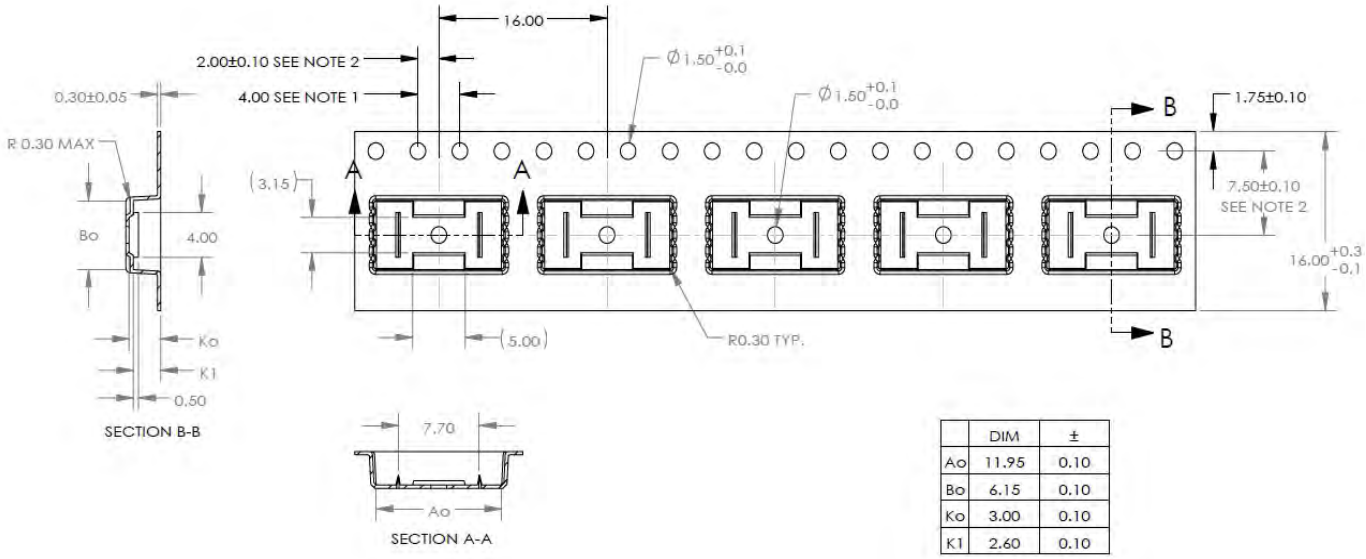
SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Tape Information



Ao	6.50 +/– 0.1
Bo	5.30 +/– 0.1
Ko	2.20 +/– 0.1
K1	1.90 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 12.2 Reel Information of SOP8(150 mil)



	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 12.3 Reel Information of SOP8(300 mil)

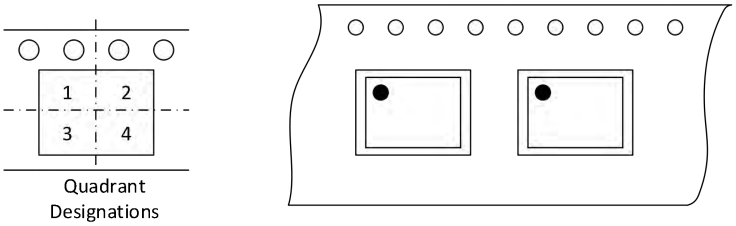


Figure 12.4 Quadrant Designation for Pin1 Orientation in Tape

13. Revision History

Revision	Description	Date
1.0	Initial version	2020/12/22
1.1	Update figure	2021/7/8
1.2	Update high voltage feature description	2021/10/28